億 都 集 團
YEEBO GROUP

SPECIFICATION
FOR
CTP MODULE

MODULE NO: YB-TG8001280S01A-C-A0

Doc.Version:00

Customer Approval:

□ Accept	□ Reject

YEEBO	NAME	SIGNATURE	DATE
Prepare	Electronic Engineer	邹伟林	2022-09-01
Check	Mechanical Engineer		2022-09-02
Verify			2022-09-02
Approval			2022-09-02

■ APPROVAL FOR SPECIFICATIONS ONLY

□ APPROVAL FOR SPECIFICATIONS AND SAMPLE

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1. Revision History

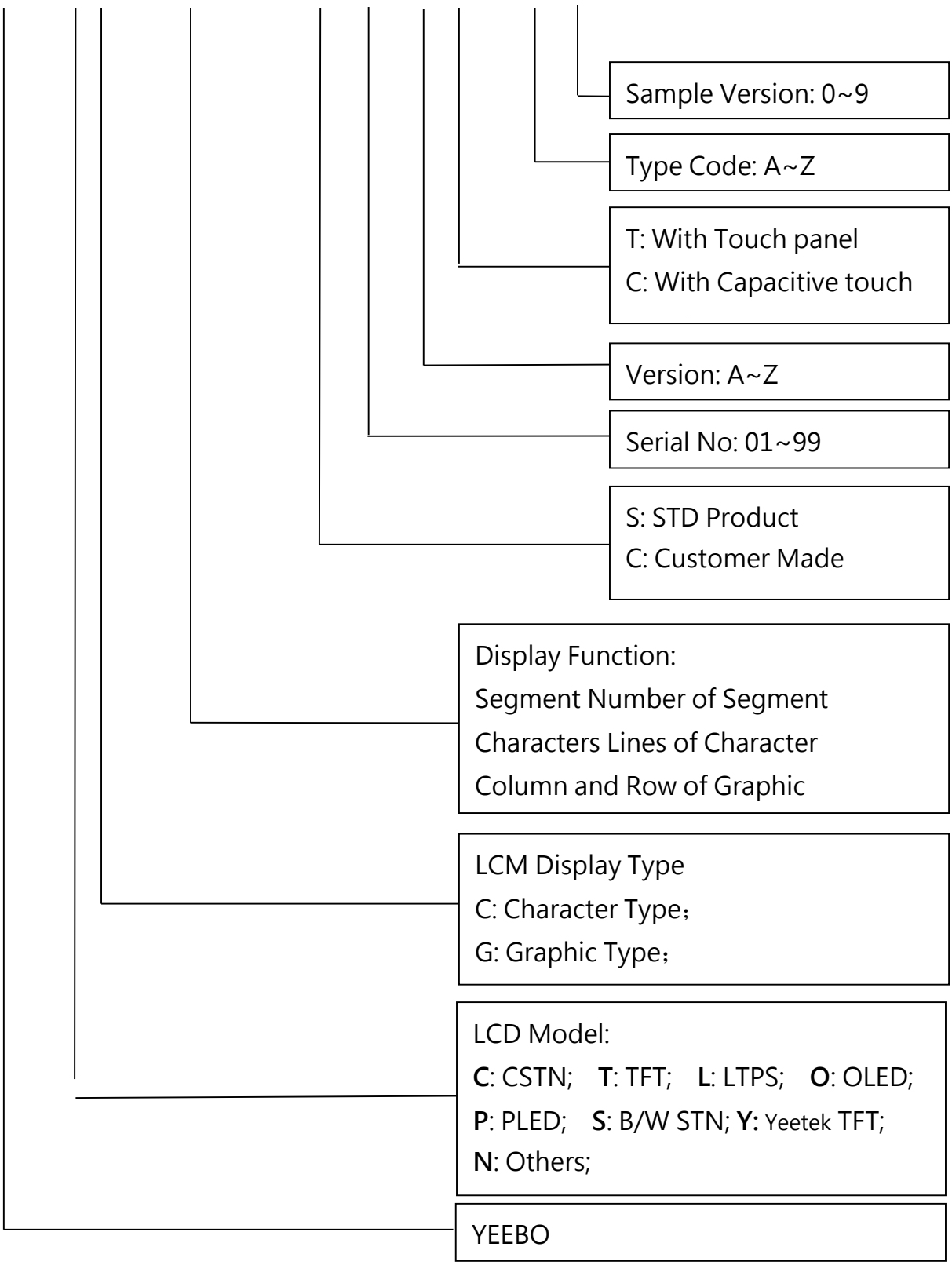
Sample Version	DOC. Version	DATE	DESCRIPTION		CHANGED BY
A0	00	2022-09-01	Spec Only	First issue	Z.W.L

2. Table of Contents:

3. Module Numbering System:

(example)

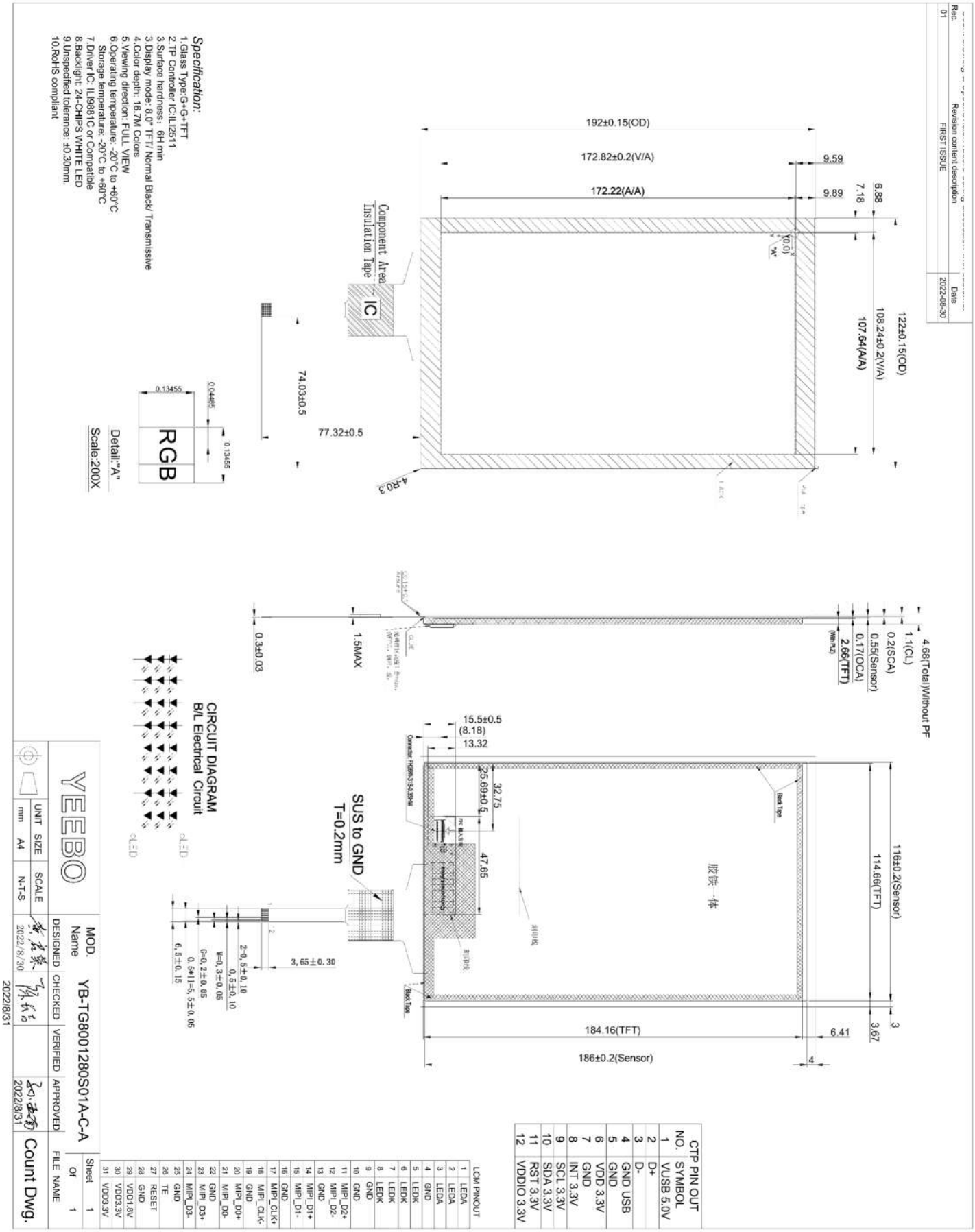
YB- TG 8001280 S 01 A-C – A 0



4. General Specification:

ITEM	SPECIFICATION
Structure	G + G + TFT
Screen Size	8.0 Inch
Display Format	800(RGB) * 1280 Pixels
Module Size(mm)	122.96 (W) * 192.00 (H) * 4.68 (T) mm
View Area(mm)	108.24(W) * 172.82(H)
Active Area(mm)	107.64(W) * 172.22(H)
Pixel Pitch(mm)	0.13455(W)×0.13455(H)
LCD Type	16.7M Color / Transmissive / Normal Black
TFT Controller IC	ILI9881C
View Angle	Free
CTP Controller IC	ILI2511
CTP Interface	USB&IIC
Weight(g)	TBD
Firmware	TBD
Test Configuration	TBD

5. Dimensional Outline:



CTP PIN OUT NO.	SYMBOL
1	VUSB 5.0V
2	D+
3	D-
4	GND USB
5	VDD 3.3V
6	GND
7	INT 3.3V
8	SCL 3.3V
9	SDA 3.3V
10	RST 3.3V
11	VDDIO 3.3V
12	

LCM PINOUT			
1	LEDA	16	GND
2	LEDA	17	MIPI_CLK+
3	LEDA	18	MIPI_CLK-
4	GND	19	GND
5	LEDK	20	MIPI_D0+
6	LEDK	21	MIPI_D0-
7	LEDK	22	GND
8	LEDK	23	MIPI_D3+
9	GND	24	MIPI_D3-
10	GND	25	GND
11	MIPI_D2+	26	TE
12	MIPI_D2-	27	RESET
13	GND	28	GND
14	MIPI_D1+	29	VDD1.8V
15	MIPI_D1-	30	VDD3.3V
		31	VDD3.3V

6. Electrical Characteristics

6-1 Absolute Maximum Ratings

6-1-1 TFT Absolute Maximum Ratings (Ta=25℃)

Item	Symbol	Min.	Type	Max.	Unit	Remark
Logic Operating Voltage	V_{DD}	-0.3	-	5.5	V	
Analog Operating Voltage	V_{DD}	-0.3	-	5.5	V	
Operating Temperature	T_{opr}	-20	-	+60	℃	
Storage Temperature	T_{stg}	-30	-	+70	℃	

Note ：Even if the absolute maximum rating of one of the above parameters is exceeded only for a short while, the quality of the product may be degraded. Therefore, be sure to use the product within the range of the absolute maximum ratings.

6-1-2 TP Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Chip power input	V_{DD}	-0.3	3.6	V
V_{DD3A} to GND	V_{DD3A}	-0.3	3.6	V
V_{DD3D} to GND	V_{DD3D}	-0.3	3.6	V
V_{DDIO} to GND	V_{DDIO}	-0.3	3.6	V
V_{DD16} to GND	V_{DD16}	-0.3	1.65	V
V_{GH} to GND	V_{GH}	-0.3	32	V
V_{TX} to GND	V_{TX}	-0.3	32	V
ESD Susceptibility HBM (Human Body Mode)**(Note 1)**	HBM		4000	V
ESD Susceptibility MM (Machine Mode)	MM		400	V

Note 1: Devices are ESD sensitive. Handling precaution is recommended.

6-2 Operating Conditions

6-2-1 TFT Operating Conditions (Ta=25℃)

Item	Symbol	Min.	Type	Max.	Unit	Remark
Analog operating voltage	VDD	2.5	2.8	3.3	V	
Digital operating voltage	VDDI	1.65	1.8	3.3	V	
Power Supply Current	IDD	-	75	112.5	mA	
Logic high level input voltage	VIH	0.7*VDDI	-	VDDI	V	
Logic low level input voltage	VIL	VSS	-	0.3*VDDI	V	
Logic high level output voltage	VOH	0.8*VDDI	-	VDDI	V	
Logic low level output voltage	VOL	VSS	-	0.2*VDDI	V	

6-2-2 TP Operating Conditions

Parameter	Symbol	Min	Max	Unit
V_{DD} to GND input power supply voltage	V_{DD}	3.14	3.46	V
V_{DD3A} to GND	V_{DD3A}	3.14	3.46	V
V_{DD3D} to GND	V_{DD3D}	3.14	3.46	V
V_{DDIO} to GND	V_{DDIO}	1.8	3.46	V
V_{GH} to GND	V_{GH}	-0.3	32	V
V_{TX} to GND	V_{TX}	-0.3	32	V
Operating Ambient Temperature Range	TA	-20	85	ºC
Operating Junction Temperature Range	TJ	-40	125	ºC
Storage Ambient Temperature Range	T_{ST}	-40	150	ºC

Note: The device is not guaranteed to function outside its operating conditions.

Table 5-3: Input Power Supply

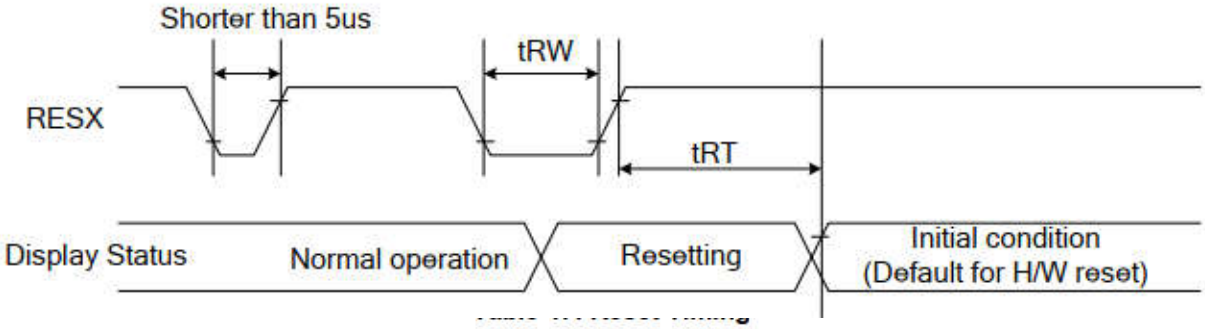
(VDD3A = VDD3D = 3.3V, Room Temperature)

Item	Symbol	Min	Typ.	Max	Unit	Condition
USB 3.3V input power supply voltage	V_{DD}	3.14	3.3	3.46	V	@ USB
Digital input power supply voltage*	V_{DD3D}	3.14	3.3	3.46	V	
Analog input power supply voltage	V_{DD3A}	3.14	3.3	3.46	V	
I/O input power supply voltage*	V_{DDIO}	1.8	3.3	3.46	V	

*If VDDIO & VDD3D is not supplied power, there is risk of I/O pin with current leakage

6-3 Timing Characteristics

6-3-1 TFT Reset Input Timing



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

6-3-2 TFT High speed mode-clock channel timing

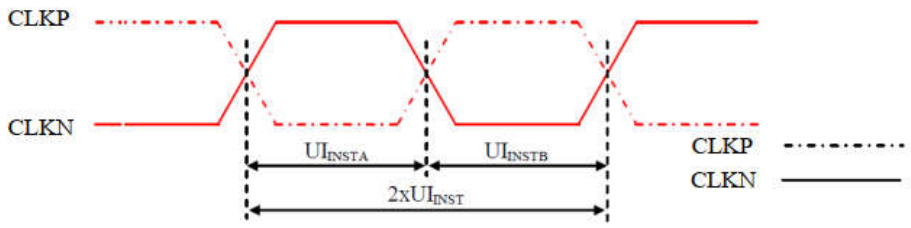


Figure 118: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
CLKP/N	UI_{INSTA}, UI_{INSTB} (Note 1)	UI instantaneous Half	2 (Note 2)	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB

2. Define the minimum value of 24 UI per Pixel, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	433 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	487 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps

6-3-3 TFT High speed mode-Data clock channel timing

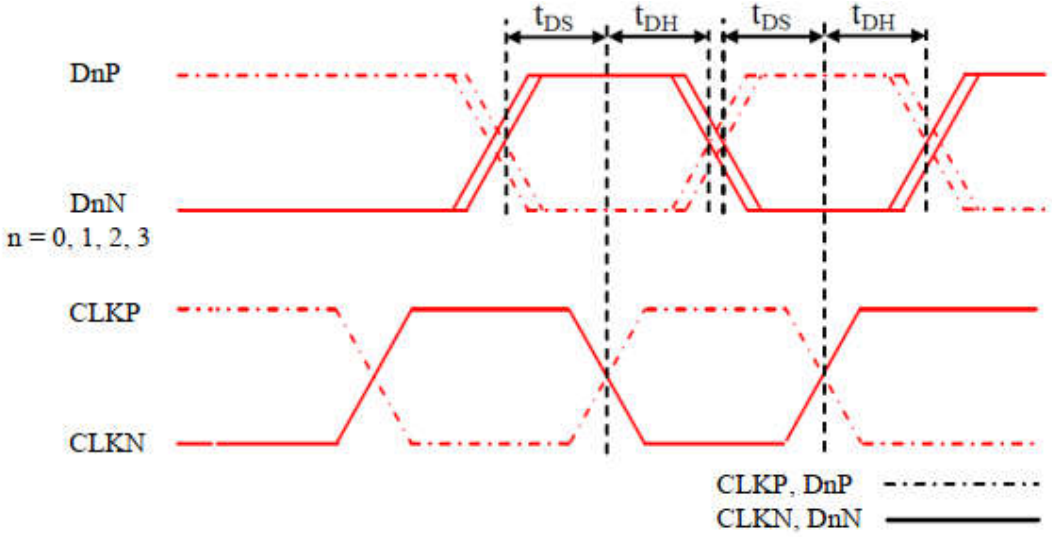


Figure 119: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

6-3-4 TFT High speed mode-Rising and falling timing

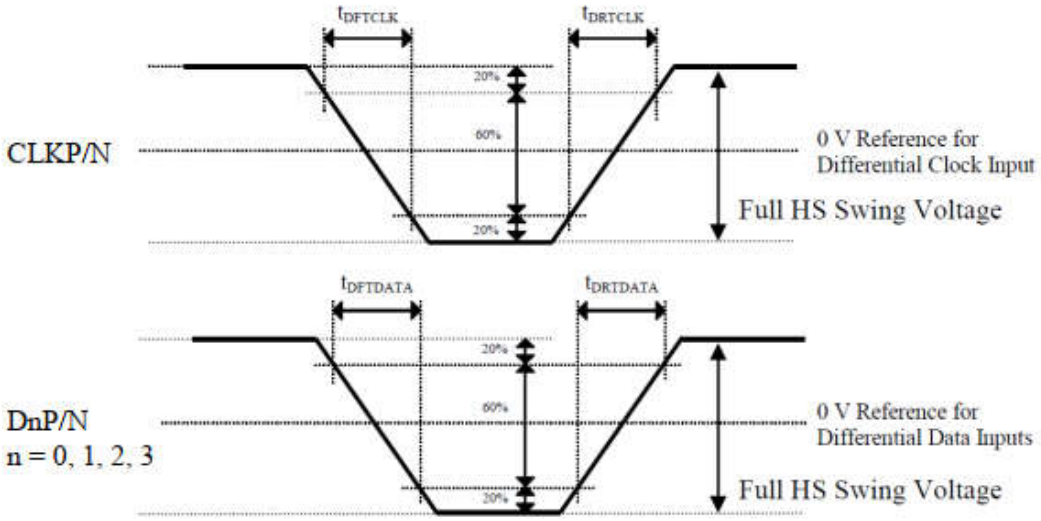


Figure 120: Rising and Falling Timings on Clock and Data Channels

Table 41: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

6-3-5 TFT Low speed mode-Bus turn around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C) are illustrated for reference purposes below.

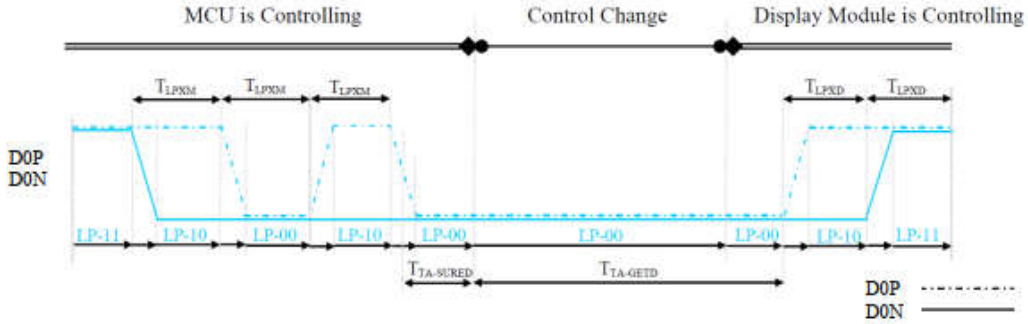


Figure 121: BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C) to the MCU are illustrated for reference purposes below.

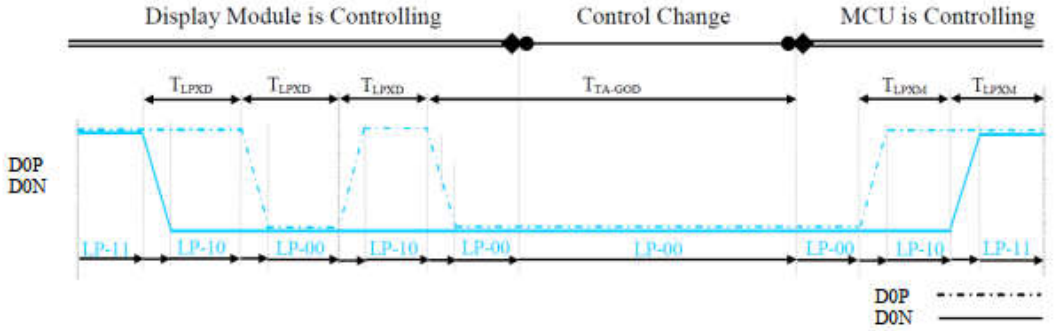


Figure 122: BTA from the Display Module to the MCU

Table 42: Low Power State Period Timings – A

Signal	Symbol	Description	Min	Max	Unit
D0P/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU ➔ Display Module (ILI9881C)	50	75	ns
D0P/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C) ➔ MCU	50	75	ns
D0P/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881C) starts driving	T_{LPXD}	$2xT_{LPXD}$	ns

Table 43: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
D0P/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881C)	$5xT_{LPXD}$	ns
D0P/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4xT_{LPXD}$	ns

6-3-6 TFT Data lanes from low power mode to high speed mode

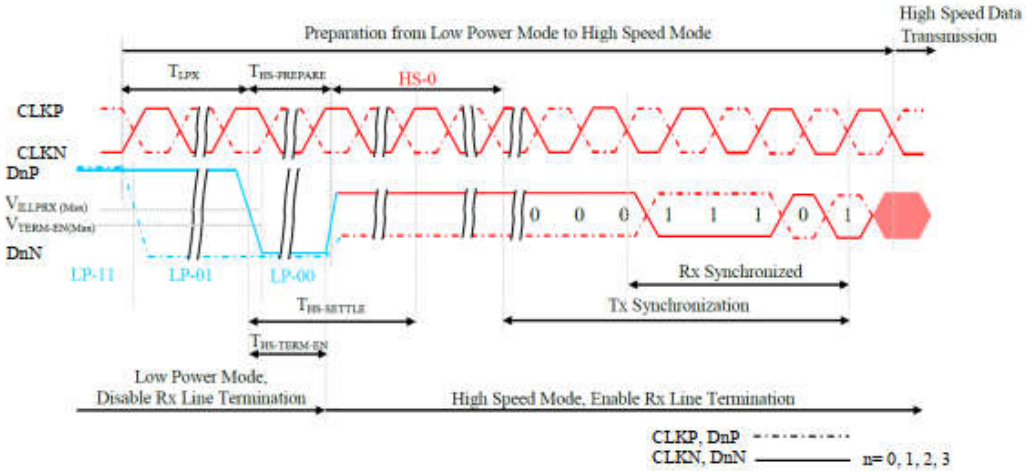


Figure 123: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

6-3-7 TFT Data lanes from high speed mode to low power mode

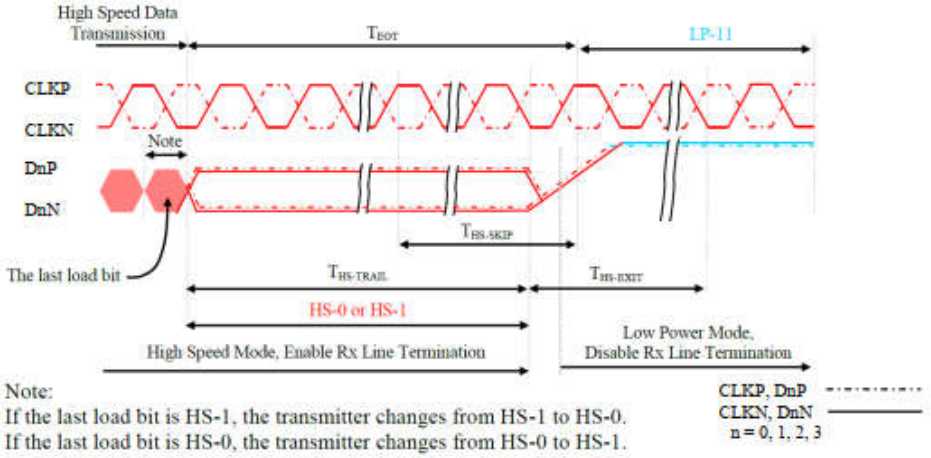


Figure 124: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

6-3-8 TFT DSI clock burst-High speed mode to/from low power mode

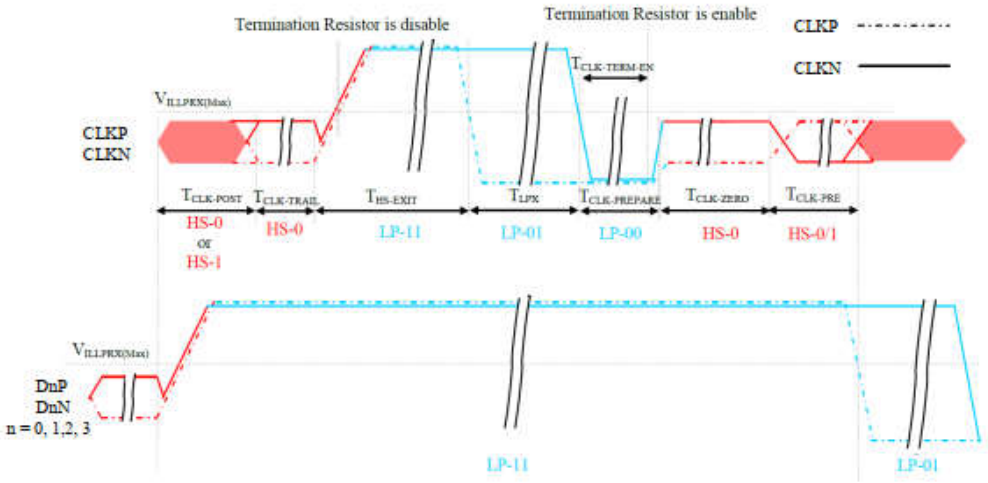
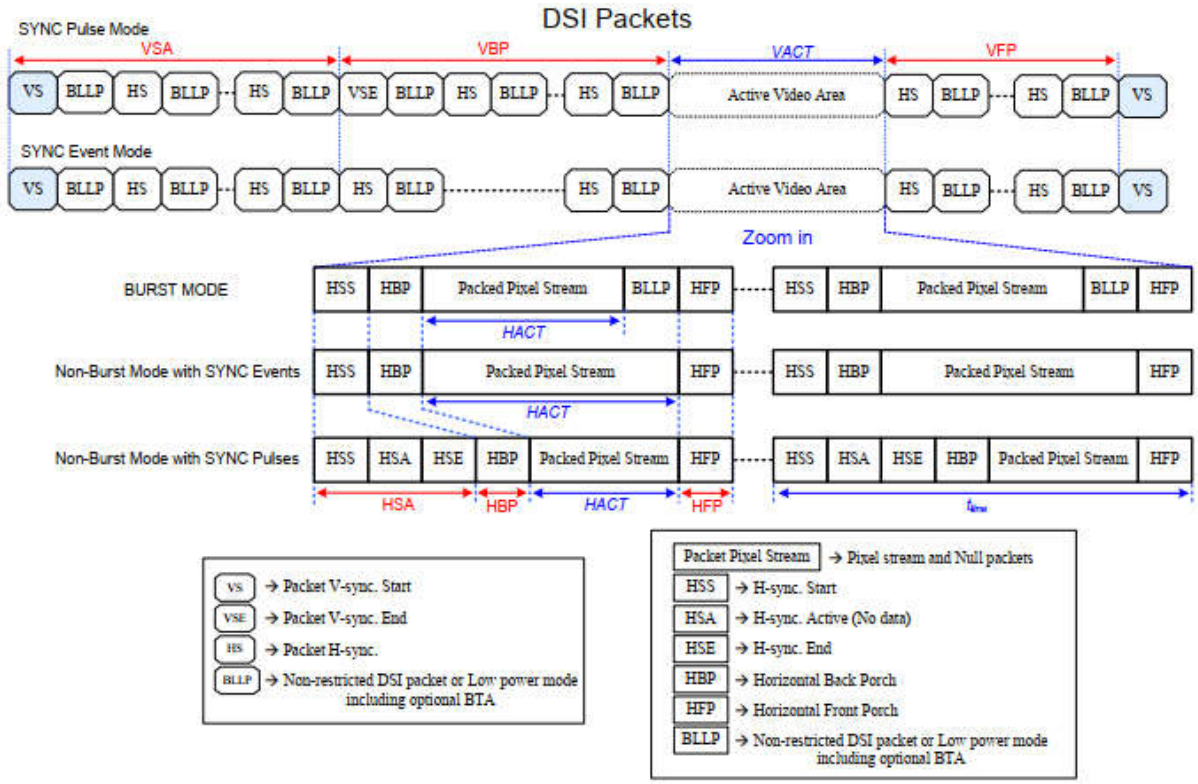


Figure 125: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

6-3-9 Timing for DSI video mode(TFT)



Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA	TBD	TBD	-	Line
Vertical Back Porch	VBP	TBD	TBD	-	Line
Vertical Front Porch	VFP	TBD	TBD	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	TBD	TBD	-	Pixel
Horizontal Back Porch	HBP	TBD	TBD	-	Pixel
Horizontal Front Porch	HFP	TBD	TBD	-	Pixel
Active pixels per line	HACT	-	800	-	Pixel
Line time	t_{line}	TBD		-	bps/lane
Bit rate	BR_{bps}	200		Note 5	Line

1 UI=1/Bit rate

HAS(pixel)= (tHSA*lane number) / (UI* pixel format)

HBP(pixel)= (tHBP*lane number) / (UI* pixel format)

HFP(pixel)= (tHFP*lane number) / (UI* pixel format)

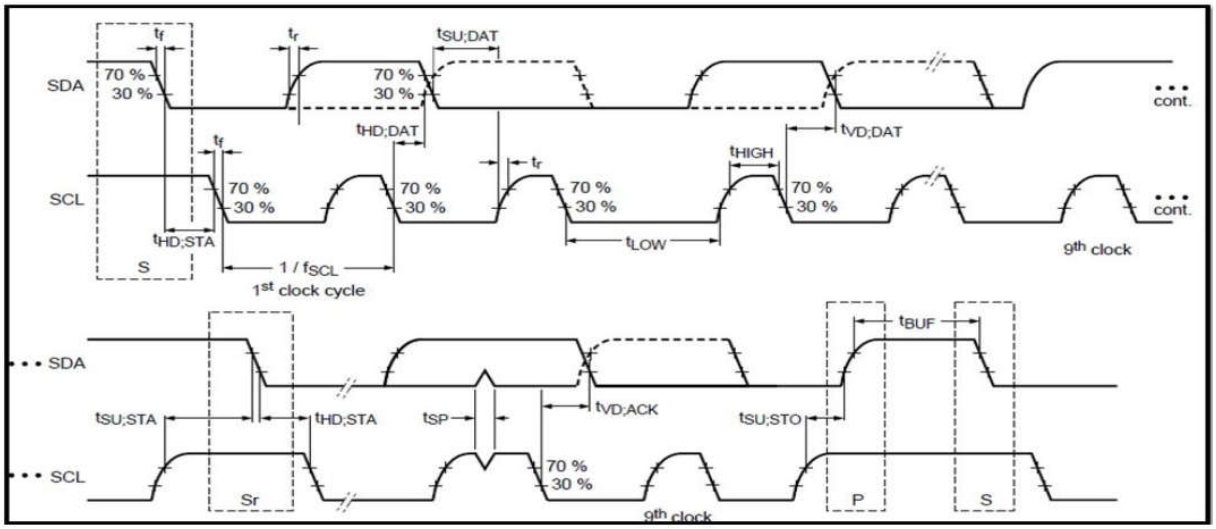
$$\text{Frame Rate} = \frac{BR_{bps} \times Lane_{num}}{(VACT+VSA+VBP+VFP) \times (HACT+HSA+HBP+HFP) \times \text{Pixel Format}}$$

Example：BR_{bps} = 457Mbps/lane, 1UI=2.1883ns, Frame rate=60Hz, VACT=1280, VSA=2, VBP=30, VFP=20, HACT=720, HSA=33, HBP=100, HFP=100, $Lane_{num}$=4(lane), Pixel Format=24(bit).

Note:

1. $Lane_{num}$: Date lane of MIPI-DSI.
2. Pixel Format: Please reference to "4.1DSI System Interface".
3. The formula exists slightly error because of the host-transmission way.
4. The best frame rate setting： 2 data lanes：50~60 Hz / 3 data lanes：50~70 Hz / 4 data lanes：50~70 Hz.
5. Please reference to "Table 39: Limited Clock Channel Speed"

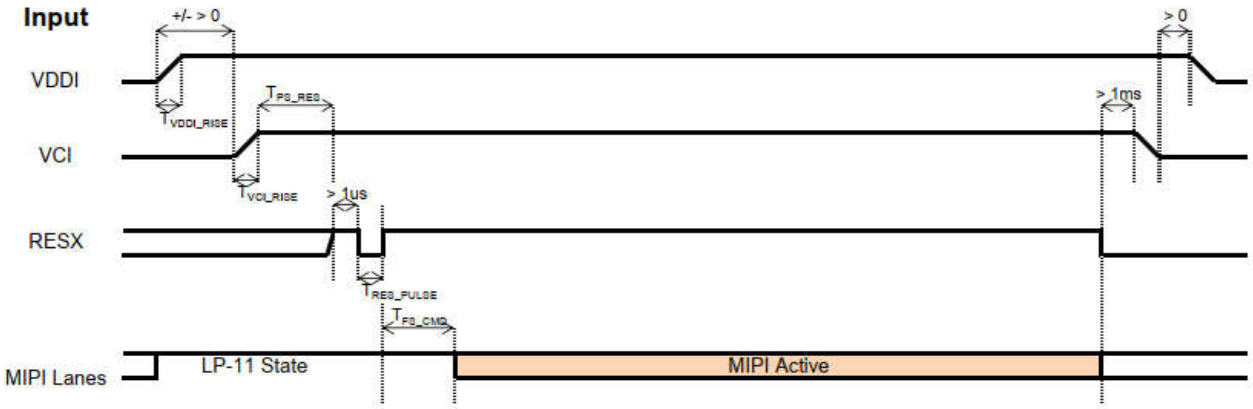
6-3-10 TP I2C AC Characteristics



Parameter	Symbol	Standard-mode		Fast-mode		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time START condition	$t_{HD;STA}$	4.0	-	0.6	-	us
LOW period of the SCL clock	t_{Low}	4.7	-	1.3	-	us
HIGH period of the SCL clock	t_{High}	4.0	-	0.6	-	us
Set-up time for a repeated START condition	$t_{SU:STA}$	4.7	-	0.6	-	us
Data hold time	$t_{HD;DAT}$	300	-	300	-	ns
Data set-up time	$t_{SU;DAT}$	250	-	100	-	ns
Rise time of both SDA and SCL signals (30% to 70%)	t_r	-	1000	20	300	ns
Fall time of both SDA and SCL signals (70% to 30%)	t_f	-	300	20	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	us
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	us
Capacitive load for each bus line	C_b	-	400	-	400	pF
Noise margin at the LOW level for each connected device	V_{nL}	$0.1V_{DD}$	-	$0.1V_{DD}$	-	V
Noise margin at the HIGH level for each connected device	V_{nH}	$0.2V_{DD}$	-	$0.2V_{DD}$	-	V

*SCL = I2C Host must to support clock stretching mode for using 400 kHz.

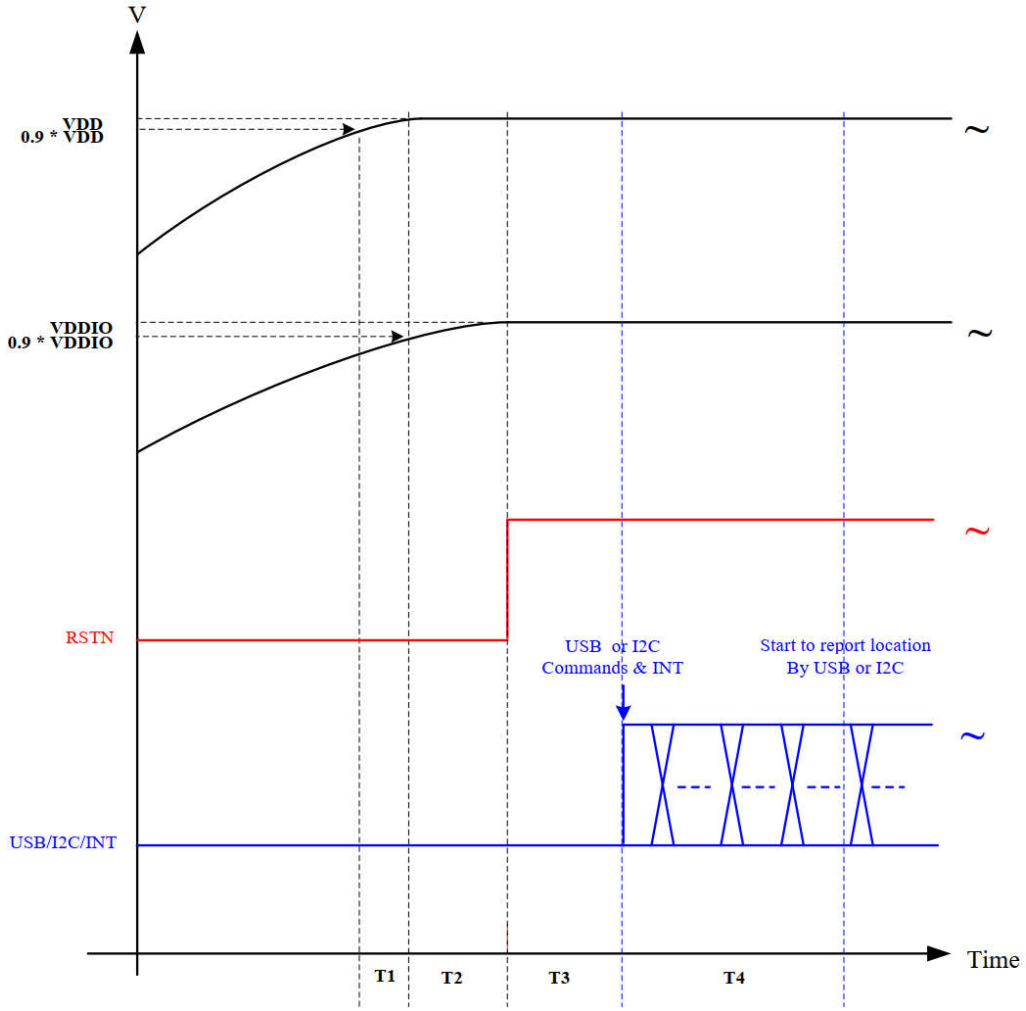
6-3-11 TFT Power ON/OFF Sequence



Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	200	-	-	us
T_{VCI_RISE}	VCI Rise time	200	-	-	us
T_{PS_RES}	VDDI/VCI on to Reset high	5	-	-	ms
T_{RES_PULSE}	Reset low pulse time	10	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

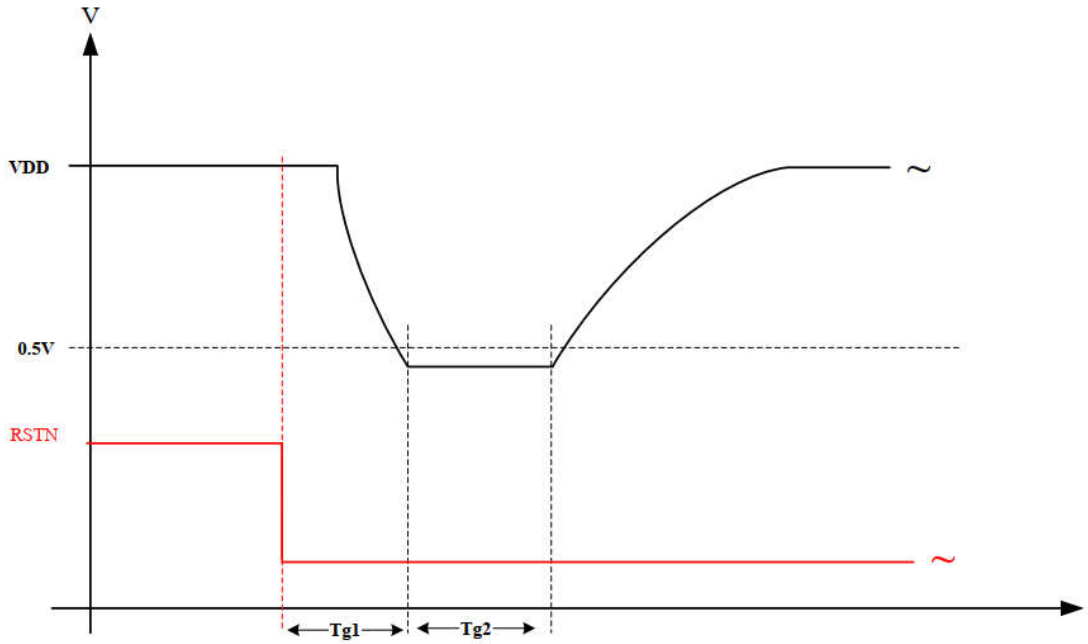
Figure 106: Power on/off sequence with Power Mode 3

6-3-12 TP Power ON Sequence



1. T1: the time difference between 0.9*VDD and 0.9*VDDIO. T1 must be ≥ 0 sec.
2. T2: the time difference between 0.9*VDDIO and RSTN. T2 must be ≥ 200 us.
3. T3: the time difference between RSTN and Commands.T3 must be ≥ 150 ms.
4. T4: IC start to report point location to host. T4 must be ≥ 300 ms.

6-3-13 TP Power-off to Power-on Sequence



Tg1 : the time difference between power-off and power-on. Tg1 must be > 10us.

Tg2 : the time difference between power-off and power-on. Tg2 must be > 10us.

Note. During the power off time, the VDD must be lower than 0.5V that make sure the touch controller have been correctly reset.

7. Optical Characteristics:

Item		Symbol	Conditions	Specifications			Unit	Note
				Min	Typ	Max		
Transmittance		T(%)	-	-	4.8	-	-	-
Contrast Ratio		CR	θ=0° Normal Viewing Angle	900	1200	-	-	(1) (2)
Response time		TR+TF		-	-	35	ms	(1) (3)
Viewing Angle	Hor.	θx+	CR≧10	-	80	-	deg.	(1)
		θx-		-	80	-		
	Ver.	θy+		-	80	-		
		θy-		-	80	-		

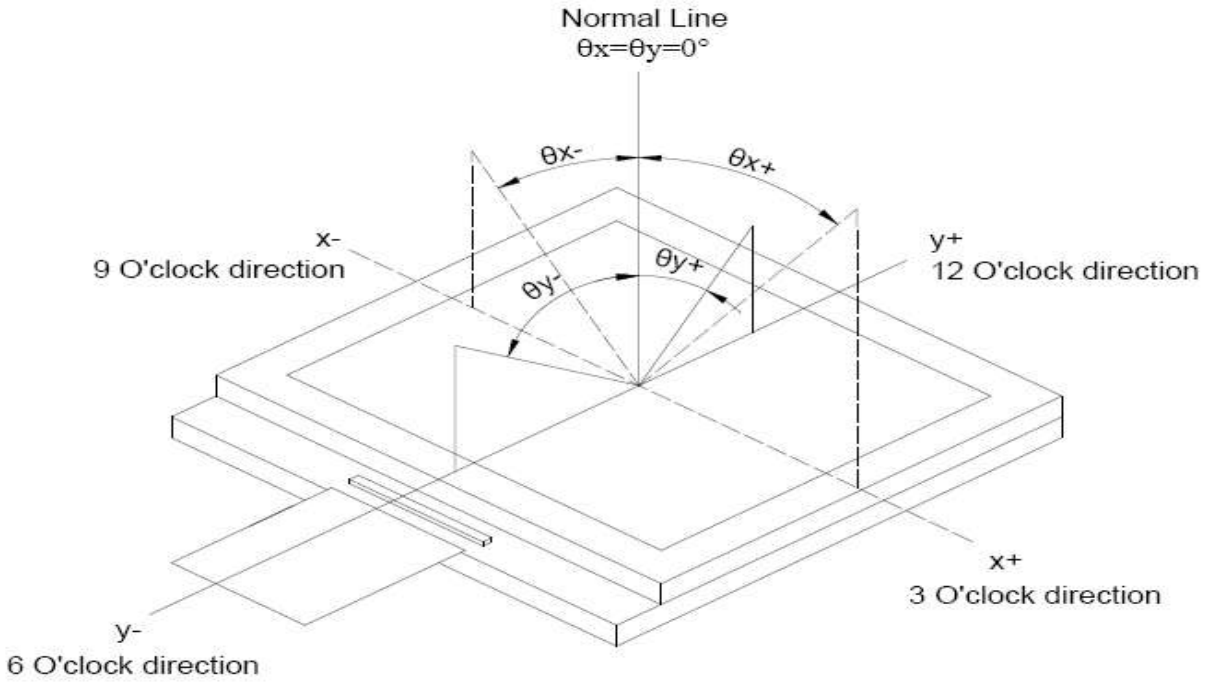
Measuring Condition
1. Measuring surrounding: dark room
2. Ambient temperature: 25±2℃
3. 30 min. Warm-up time.

Color of CIE Coordinate:

(Ta=25℃)

Item		Symbol	Condition	Min.	Typ.	Max.
Chromaticity Coordinates (Transmissive)	Red	x	θ = φ = 0° LED Backlight	TBD	(0.646)	TBD
		y		TBD	(0.339)	TBD
	Green	x		TBD	(0.271)	TBD
		y		TBD	(0.581)	TBD
	Blue	x		TBD	(0.138)	TBD
		y		TBD	(0.158)	TBD
	White	x		TBD	(0.306)	TBD
		y		TBD	(0.360)	TBD

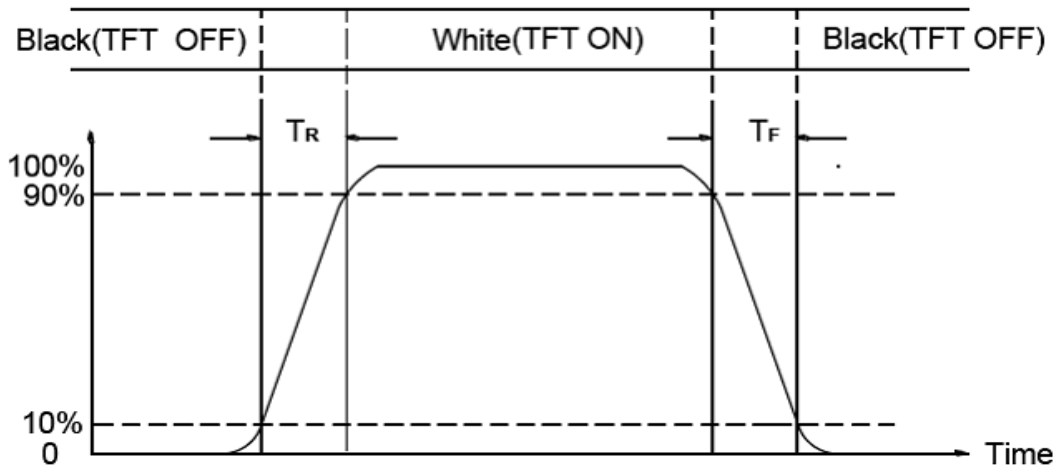
Note (1) Definition of Viewing Angle :



Note (2) Definition of Contrast Ratio(CR) :
measured at the center point of panel

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black}}$$

Note (3) Definition of Response Time : Sum of TR and TF



8. Interface Pin Assignment:

8-1 TFT Pin Assignment

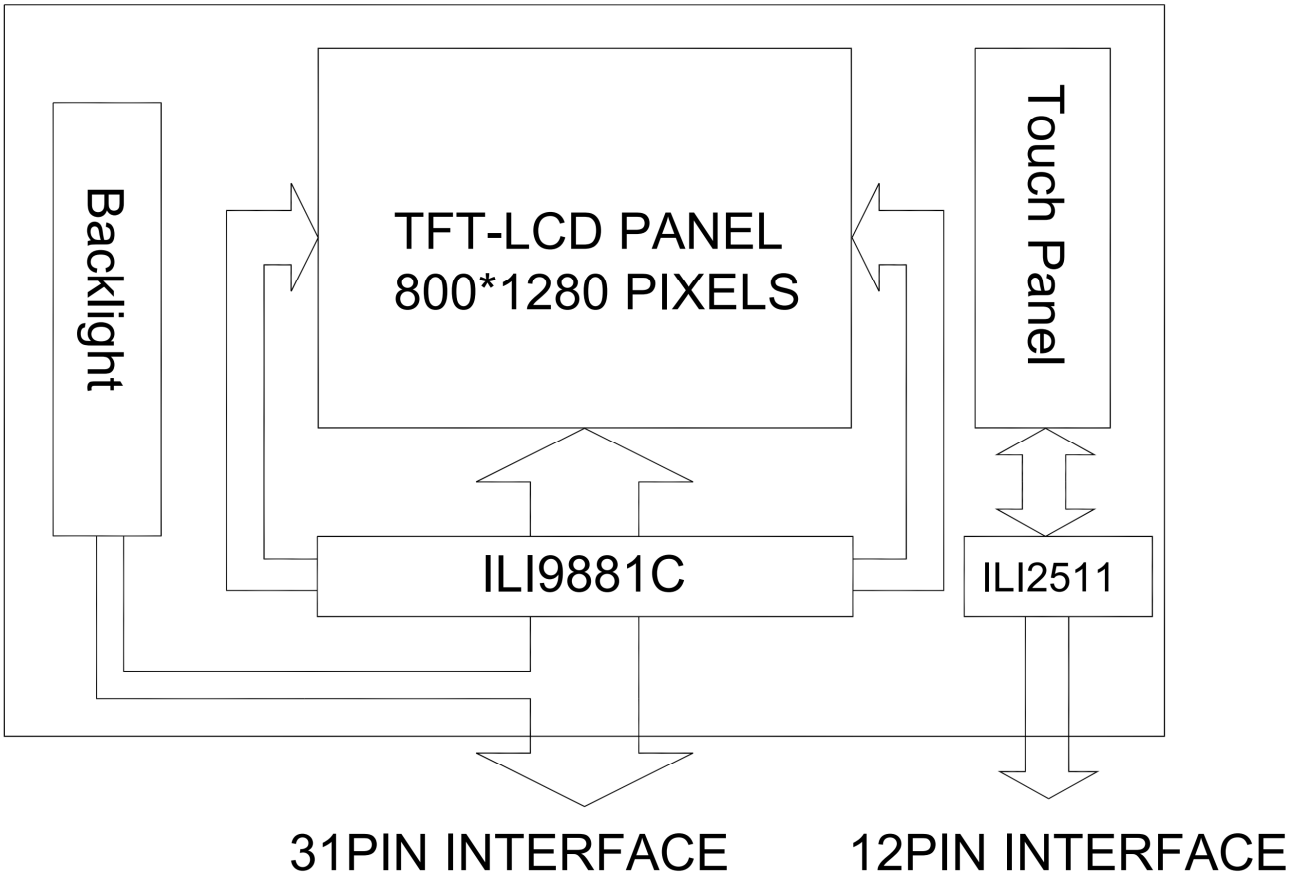
No.	Symbol	Function
1~3	LEDA	Power for LED backlight (Anode)
4	GND	Ground
5~8	LEDK	Power for LED backlight (Cathode)
9	GND	Ground
10	GND	Ground
11	D2P	High speed interface data differential signal input/output pins
12	D2N	High speed interface data differential signal input/output pins
13	GND	Ground
14	D1P	High speed interface data differential signal input/output pins
15	D1N	High speed interface data differential signal input/output pins
16	GND	Ground
17	CP	High speed interface CLOCK differential signal input pins
18	CN	High speed interface CLOCK differential signal input pins
19	GND	Ground
20	D0P	High speed interface data differential signal input/output pins
21	D0N	High speed interface data differential signal input/output pins
22	GND	Ground
23	D3P	High speed interface data differential signal input/output pins
24	D3N	High speed interface data differential signal input/output pins
25	GND	Ground
26	TE	Tearing effect output pin
27	RESET	Reset pin
28	GND	Ground
29	IOVCC	Power supply for logic circuit.
30	VCI	Power supply for analog circuit
31	VCI	Power supply for analog circuit

8-2 TP Pin Assignment

Symbol	Description
P	Power pad
CLK	Clock
I	Input only
O	Output only (Push-pull)
I/O	input / output pad

No.	Name	Type	Description
1	VUSB 5.0V	P	USB 5V input power supply
2	D+	I/O	USB interface
3	D-	I/O	USB interface
4	GND	P	Connect to system ground
5	GND	P	Connect to system ground
6	VDD 3.3V	P	3.3V input power supply
7	GND	P	Connect to system ground
8	INT	I/O	Interrupt output
9	SCL	I/O	I2C interface, clock input
10	SDA	I/O	I2C interface, data input
11	RST	I/O	External hardware reset input
12	VDDIO	P	1.8V/3.3V input power supply for I2C, SPI, UART, GPIO

9. Block Diagram:



10. Backlight:

1. Standard Lamp Styles (Edge Lighting Type):
   The LED chips are distributed over the edge light area of the illumination unit, which gives the less power consumption:

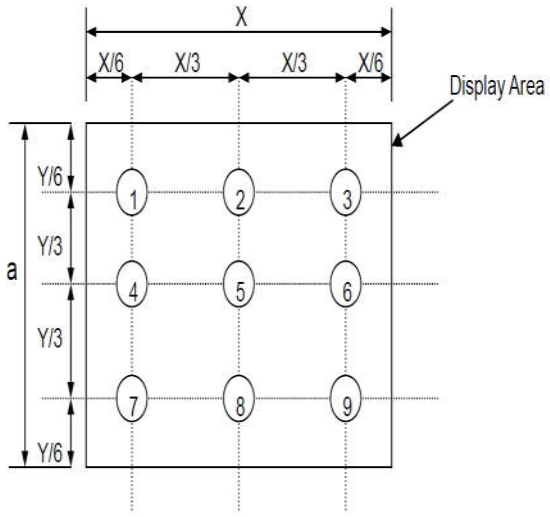
2. The Main Advantages of the LED Backlight are as following:
   2.1 The brightness of the backlight can simply be adjusted.
   By a resistor or a potentiometer.

3. Data About LED Backlight: (Ta=25°)

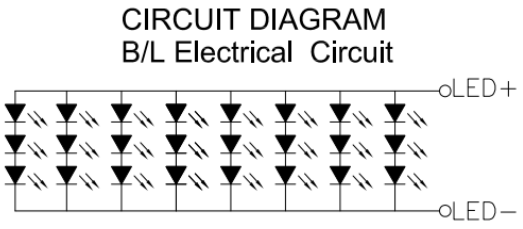
PARAMETER	Sym.	Min.	Typ.	Max.	Unit	Test Condition	Note
Supply Current	I		160		mA	If=160mA	-
Supply Voltage	V	8.1	9.6	10.2	V		-
Luminous Intensity for LCM	IV	400	450	-	cd/m2		2
Uniformity for LCM	-	70	-	-	%		3
Life Time	-	20000	-	-	Hr.		4
Color	White						

NOTE:
1. Operating temperature 25°C, humidity 50%.
2. Average Luminous Intensity of P1-P9
3. Uniformity = Min/Max * 100%
4. LED life time defined as follows: The final brightness is at 50% of original brightness

Measured Method: (X*Y: Light Area)



Internal Circuit Diagram



Using aperture of 1°, distance 50cm.

11. Standard Specification for Reliability :

11–1. Standard Specifications for Reliability

No	Item	Description
01	High temperature operation	The sample should be allowed to stand at 60℃ for 240 hours under driving condition and then returning it to normal temperature condition, and allowing it stand for 2 hours.
02	Low temperature operation	The sample should be allowed to stand at -20℃ for 240 hours under driving condition and then returning it to normal temperature condition, and allowing it stand for 2 hours.
03	High temperature storage	The sample should be allowed to stand at 60℃ for 240 hours under no-load condition, and then returning it to normal temperature condition, and allowing it stand for 2 hours.
04	Low temperature storage	The sample should be allowed to stand at -20℃ for 240 hours under no-load condition, then returning it to normal temperature condition, and allowing it stand for 2 hours.
05	Moisture storage	The sample should be allowed to stand at 60℃,90%RH MAX for 240 hours under no-load condition, then taking it out and drying it at normal temperature for 2 hours.
06	Thermal shock storage	The sample should be allowed to stand the following 10 cycles : -20℃ for 30 minutes → normal temperature for 5 minutes → +60℃ for 30 minutes → normal temperature for 5 minutes, as one cycle.
07	Packing vibration	Frequency range : 10Hz ~ 55Hz Amplitude of vibration : 1.5mm Sweep time: 12 min X,Y,Z 2 hours for each direction.
08	Packing drop test	According to ISTA 1A 2001.
09	Electrical Static Discharge	Air: ±6KV 150pF/330Ω 5 times
		Contact: ±4KV 150pF/330Ω 5 time

*Sample size for each test item is 3~5pcs

11 - 2. Testing Conditions and Inspection Criteria

For the final test the testing sample must be stored at room temperature for 24 hours, after the tests listed in Table 11-1, Standard specifications for Reliability have been executed in order to ensure stability.

No	Item	Test Model	In section Criteria
01	Current Consumption	Refer To Specification	The current consumption should conform to the product specification.
02	Contrast	Refer To Specification	After the tests have been executed, the contrast must be larger than half of its initial value prior to the tests.
03	Appearance	Visual inspection	Defect free.

11- 3. MTBF

MTBF	Functions, performance, appearance, etc. shall be free from remarkable deterioration within 50,000 hours under ordinary operating and storage conditions room temperature (25±5℃), normal humidity (50±10% RH), and in area not exposed to direct sun light.

12. Specification of Quality Assurance:

12-1. Purpose

This standard for Quality Assurance should affirm the quality of LCD module products to supply to purchaser by YEEBO CORPORATION (Supplier).

12-2. Standard for Quality Test

a. Inspection:

Before delivering, the supplier should take the following tests, and affirm the quality of product.

b. Electro-Optical Characteristics:

According to the individual specification to test the product.

c. Test of Appearance Characteristics:

According to the individual specification to test the product.

d. Test of Reliability Characteristics:

According to the definition of reliability on the specification for testing products.

e. Delivery Test:

Before delivering, the supplier should take the delivery test.

(i) Test method: According to **ISO2859-1.**General Inspection Level Ⅱ take a single time.

(ii) The defects classify of AQL as following:

Major defect: AQL = 0.65

Minor defect: AQL = 2.5

Total defects: AQL = 2.5

12-3. Non- conforming Analysis & Deal With Manners

a. Non- conforming Analysis:

(i) Purchaser should supply the detail data of non- conforming sample and the non-conforming.

(ii) After accepting the detail data from purchaser, the analysis of non- conforming should be finished in two weeks.

(iii) If supplier can not finish analysis on time, must announce purchaser before 3 days.

b. Disposition of non- conforming:

(i) If find any product defect of supplier during assembly time, supplier must change the good product for every defect after recognition.

(ii) Both supplier and customer should analyze the reason and discuss the disposition of non- conforming when the reason of nonconforming is not sure.

12-4. Agreement items

Both sides should discuss together when the following problems happen.

a. There is any problem of standard of quality assurance, and both sides should think that must be modified.

b. There is any argument item which does not record in the standard of quality assurance.

c. Any other special problem.

12-5. Standard of The Product Appearance Test

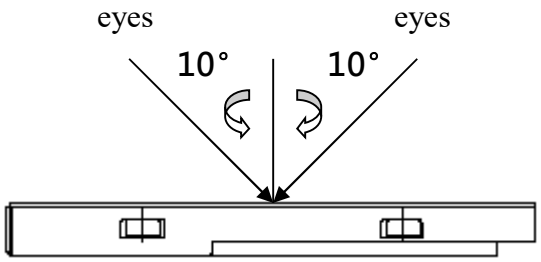
a. Manner of appearance test:

(i) The test must be under 20W × 2 or 40W fluorescent light, and the distance of view must be at 30±5cm.

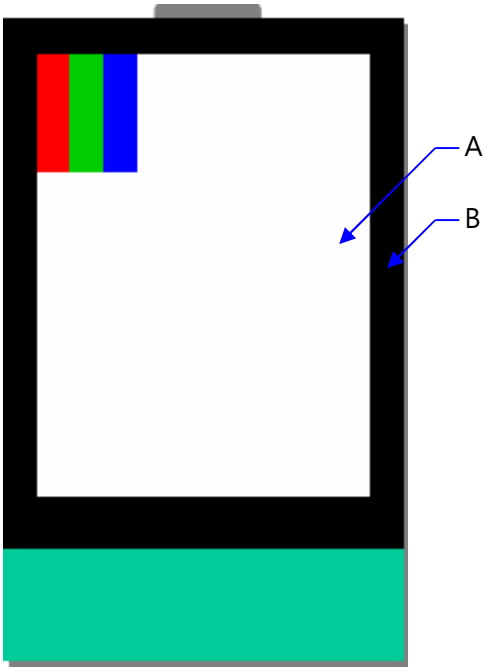
(ii) When test the model of transmissive product must add the reflective plate.

(iii)The test direction is base on around 10° of vertical line.

(iiii)Temperature: 25±5℃ Humidity: 60±10%RH



(iv) Definition of area:



A. Area: Viewing area.

B. Area: Out of viewing area.
(Outside viewing area)

b. Basic principle:

(i) It will accord to the AQL when the standard can not be described.

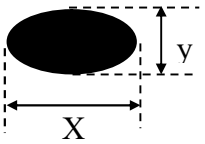
(ii) The sample of the lowest acceptable quality level must be discussed by both supplier and customer when any dispute happened.

(iii) Must add new item on time when it is necessary.

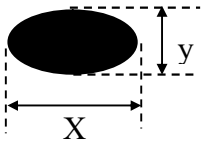
c. Standard of inspection: (Unit: mm)

12-6. Inspection specification

Defect out of viewing area can be neglected.

<table>
<tr><th>Item</th><th>Specification Unit : mm</th><th>AQL</th></tr>
<tr><td>Electrical Testing</td><td>1.1 Open
1.2 Short
1.3 T/P failure
1.4 Missing vertical, horizontal segment, segment contrast defect.
1.5 Missing character, dot or icon.
1.6 Display malfunction.
1.7 No function or no display.
1.8 Current consumption exceeds product specifications.
1.9 LCD viewing angle defect.
1.10 Mixed product types.
1.11 Flicker</td><td>0.65</td></tr>
<tr><td>explosion-proof film bubble/Concave and convex point/indentation / Contamination</td><td>
<table>
<tr><th>D</th><th>Acceptable numbers</th></tr>
<tr><td>≤0.3</td><td>ignored (No more than five spots within 5mm G)</td></tr>
<tr><td>0.3≤D≤0.5</td><td>4</td></tr>
<tr><td>0.5＜D≤1.0</td><td>2</td></tr>
<tr><td>1.0＜D≤1.5</td><td>2</td></tr>
<tr><td>D＞1.5</td><td>NG</td></tr>
</table>


D=(x+y)/2
1、 Product’s front side checked according to this specification, back side ignored, but light leakage is not allowed.
2、 Printing ink peel off is not allowed.
3、 The particle will be ignored when it is removable by cleaning
* Densely spaced: No more than two spots within 10mm</td><td>2.5</td></tr>
</table>

<table>
<tr>
<td>Black spots / White spots /Bright spots/ Color spots /polluted inside/ punctured</td>
<td>
<table>
<tr><th>D</th><th>Acceptable numbers</th></tr>
<tr><td>≤0.2</td><td>ignored (No more than five spots within 5mm)</td></tr>
<tr><td>0.2≤D≤0.4</td><td>4</td></tr>
<tr><td>0.4<D≤0.8</td><td>3</td></tr>
</table>


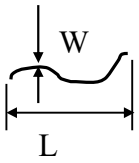
D=(x+y)/2

1、Product’s front side checked according to this specification, back side ignored, but light leakage is not allowed.

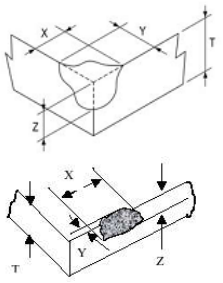
2、Printing ink peel off is not allowed.

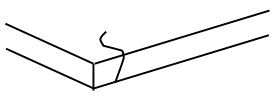
3、The particle will be ignored when it is removable by cleaning

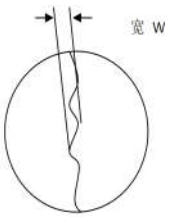
4、Not visible through 5% ND filter

* Densely spaced: No more than two spots within 10mm
</td>
<td>2.5</td>
</tr>
<tr>
<td>Linear Object: Fiber, scurf, scratches and other linear defects (not affecting function)</td>
<td>
<table>
<tr><th>W</th><th>L</th><th>Acceptable numbers</th></tr>
<tr><td>≤0.05</td><td>≤8</td><td>ignored No more than five lines within 5mm)</td></tr>
<tr><td>0.1<W≤0.3</td><td>≤8</td><td>2</td></tr>
<tr><td>W〉0.3</td><td></td><td>NG</td></tr>
</table>


The reverse side scratches, not affect to the electronic circuit, cannot find the scratches from the front side is acceptable

* Densely spaced: No more than two lines within 10mm
</td>
<td>2.5</td>
</tr>
<tr>
<td>Glass edge chipping、edge breakage</td>
<td>
<table>
<tr><th colspan="2">Edge breakage can’t affect visual effection (edge breakage can’t cause damage to circuit); over lens have no visual damage</th></tr>
<tr><th>conditions</th><th>Acceptable numbers</th></tr>
<tr><td>X≤3mm,Y≤2mm, Z≤T</td><td>5</td></tr>
</table>


</td>
<td>2.5</td>
</tr>
<tr>
<td>Glass broken</td>
<td>Visual broken is NG, and there is no potential fault.
 </td>
<td>0.65</td>
</tr>
</table>

<table>
<tr><td colspan="2">1. V/A printed edges sawtooth inspected according to this standard
2. LOGO’s sawtooth</td><td>Some contentious defect judged according to samples
<table><tr><td>Product type</td><td>Conditions</td></tr><tr><td>Same size</td><td>1、width below 0.2 inch（included）ignored，above 0.2 NG
2、Length not accounted</td></tr></table></td><td> 
</td><td>2.5</td></tr>
<tr><td colspan="2">Specific dimension</td><td>In accordance with product outline drawing or specification (key dimension) or engineering sample.</td><td></td><td>2.5</td></tr>
<tr><td colspan="2">Glue overflow/Frame</td><td>1. Glue overflow exceed 0.2mm to the black frame is not allowed.
  </td><td></td><td>2.5</td></tr>
<tr><td rowspan="3">FPC</td><td>Bonding bubble/ Misalignment</td><td>FPC golden finger hot pressure’s bubble or impurity diameter shall be below 1/2 of the pressed area, pressed deviation shall not exceed 1/2 of the silver line width, and 40X microscope cannot have obvious cracks.</td><td></td><td>0.65</td></tr>
<tr><td>Folded mark（minor fault）</td><td>Linearity irreversibility folded mark and acute angle folded mark is NG.</td><td></td><td>2.5</td></tr>
<tr><td>EMI FILM（minor fault）</td><td>Surface broken, scratched≦0.3mm
Surface broken below 5mm can be modified by print ink, after modified, the result shall be achieved to EMI</td><td></td><td>2.5</td></tr>
</table>

13. Handling Precaution:

13-1 Handling of LCM

- Don't give external shock.
- Don't apply excessive force on the surface.
- Liquid in LCD is hazardous substance. Must not lick and swallow. when the liquid is attach to your hand, skin, cloth etc. Wash it out thoroughly and immediately.
- Don't operate it above the absolute maximum rating.
- Don't disassemble the LCM.
- The operators should be grounded whenever he/she comes into contact with the module. Never touch any of the conductive parts such as the LSI pads,the copper leads on the PCB and the interface terminals with any parts of the human body.
- The modules should be kept in antistatic bags or other containers resistant to static for storage.
- The module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

13-2 Storage

- Store in an ambient temperature of 25±10℃, and in a relative humidity of 50±10%RH. Don't expose to sunlight or fluorescent light.
- Storage in a clean environment, free from dust, active gas, and solvent.
- Store in anti-static electricity container.
- Store without any physical load.

13-3 Soldering

- Use only soldering irons with proper grounding and no leakage.
- Iron: No higher than 310±10℃ and less than 3 sec during Hand soldering.
- Rewiring: no more than 2 times.

14. Warranty

This product has been manufactured to specifications as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we will not take responsibility if the product is used in medical devices, nuclear power control equipment, aerospace equipment, fire and security systems, or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required. If the product is to be used in any of the above applications, we will need to enter into a separate product liability agreement.

1. We cannot accept responsibility for any defect arise after additional process of the product (including disassembly and reassembly), after product delivery.
2. We cannot accept responsibility for any defect, which may arise after the application of strong external force to the product.
3. We cannot accept responsibility for any defect, which may arise due to the application of static electricity after the product has passed your company's acceptance inspection procedures.
4. We can not accept responsibility for industrial property, which may arise through the use of your product , with exception to those issues relating directly to the structure or method of manufacturing of our product within one year from YEEBO shipment.
5. For Heatseal Product which required to heatseal by customer side, parts must be used within three months after delivery from factory.
6. For TAB Product which required to solder by customer side, parts must be used within three months after delivery from factory.
7. The liability of YB is limited to repair or replacement on the terms set forth below. YB will not be responsible for any subsequent or consequential events or injury or damage to any personnel or user including third party personnel and/or user. Unless otherwise agreed in writing between YB and the customer, YB will only replace or repair any of its LCD which is found defective electrically or visually when inspected in accordance with YB GENERAL LCD INSPECTION STANDARD.

15. Guarantee:

Our products meet requirements of the environment.
YEEBO ROHS requirement is based on European Union Directive 2011/65/EU(ROHS) Requirements and Update.