億 都 集 團
YEEBO GROUP

SPECIFICATION
FOR
CTP MODULE

MODULE NO: YB-TG4001280S01A-C-A0

Doc.Version:00

Customer Approval:

□ Accept	□ Reject

YEEBO	NAME	SIGNATURE	DATE
Prepare	Electronic Engineer	邹伟林	2022-09-01
Check	Mechanical Engineer		2022-09-02
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Approval			2022-09-02

■ APPROVAL FOR SPECIFICATIONS ONLY

□ APPROVAL FOR SPECIFICATIONS AND SAMPLE

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1. Revision History

Sample Version	DOC. Version	DATE	DESCRIPTION		CHANGED BY
A0	00	2022-09-01	Spec Only	First issue	Z.W.L

2. Table of Contents:

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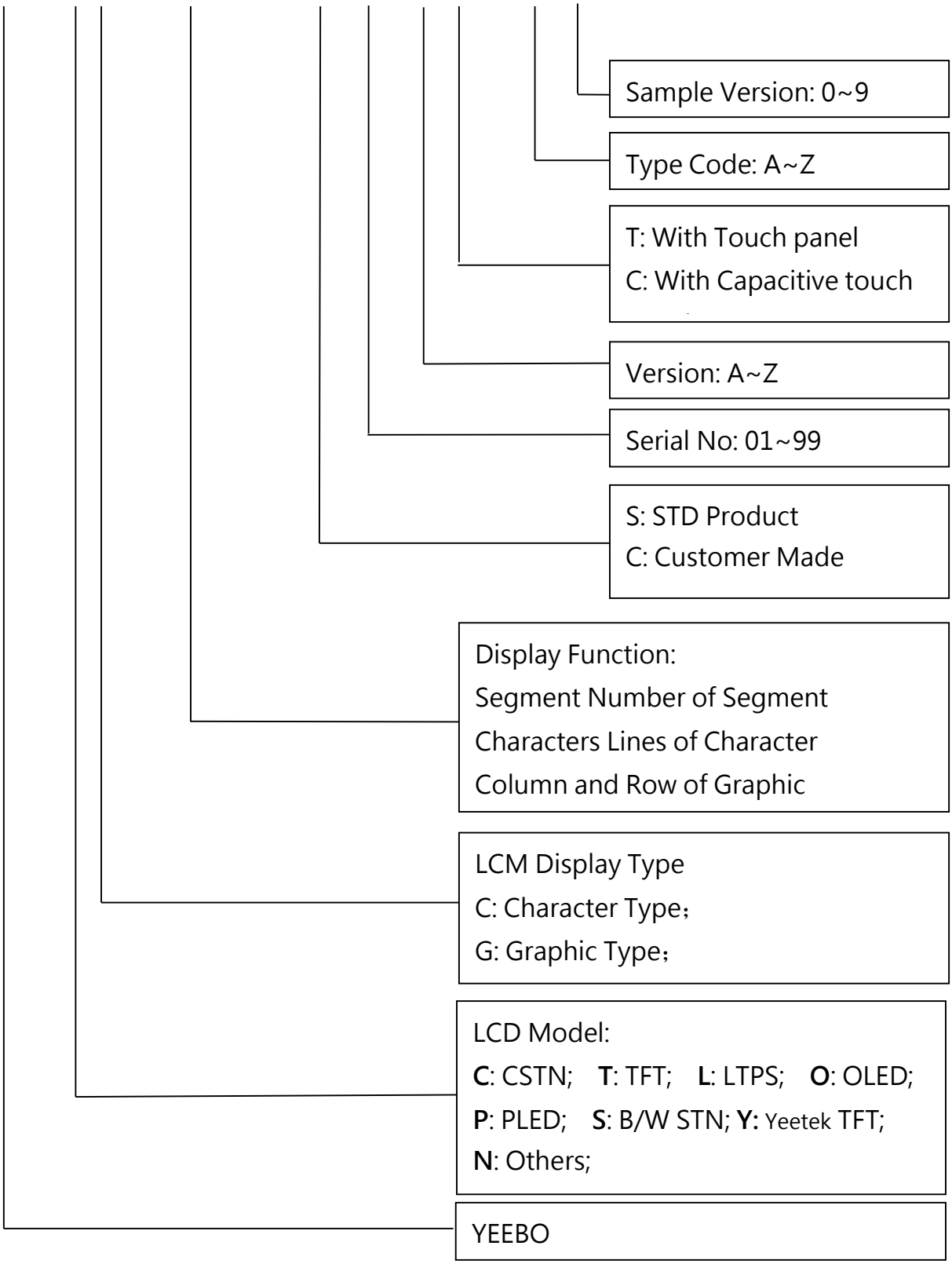
3. Module Numbering System:

(example)

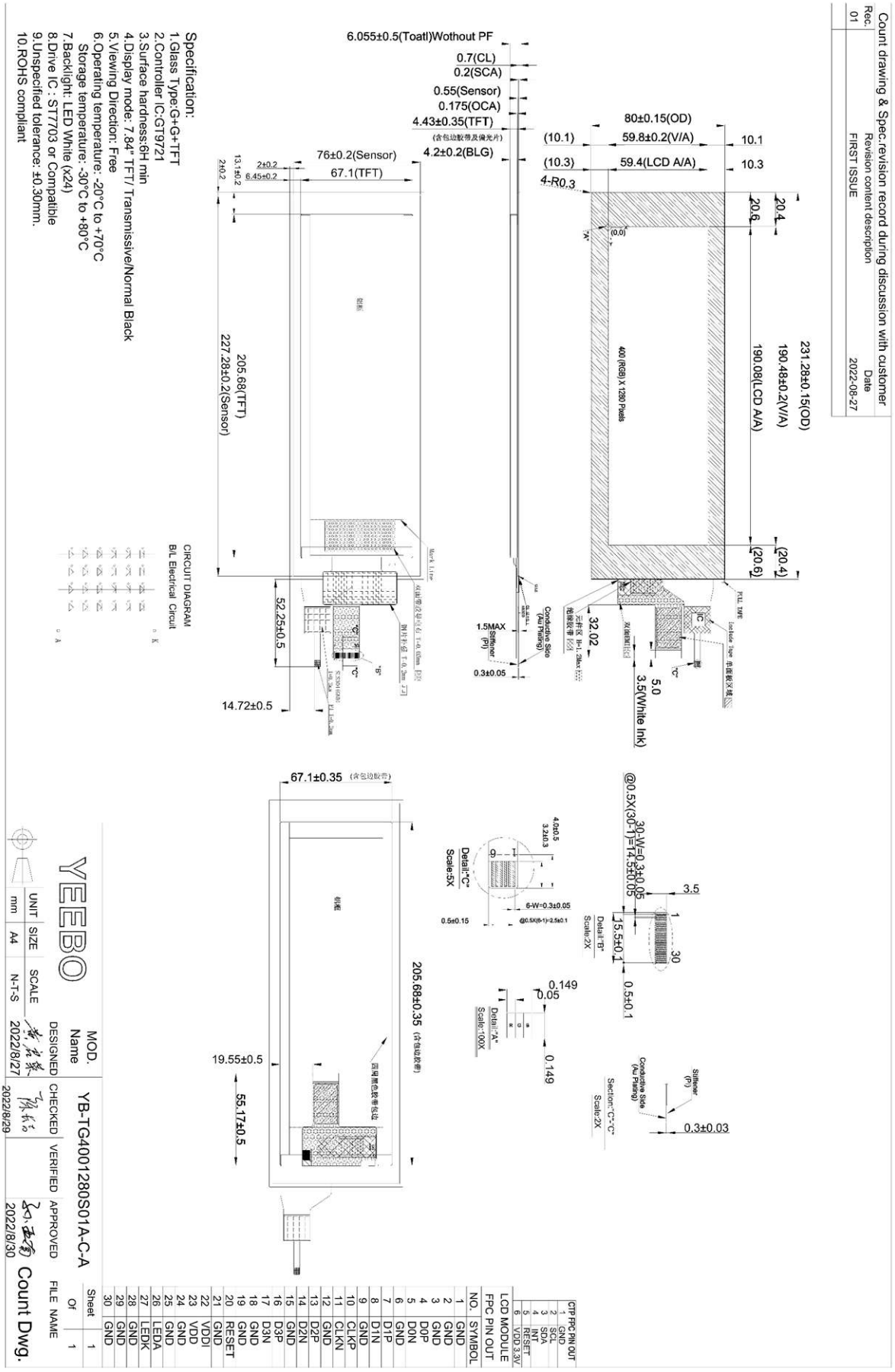
YB- TG 4001280 S 01 A-C – A 0



4. General Specification:

ITEM	SPECIFICATION
Structure	G + G + TFT
Screen Size	7.84 Inch
Display Format	400(RGB) * 1280 Pixels
Module Size(mm)	231.28 (W) * 80.00 (H) * 6.05 (T) mm
View Area(mm)	59.80 (W) * 190.48 (H)
Active Area(mm)	59.40 (W) * 190.08 (H)
Pixel Pitch(mm)	0.1485 (W) × 0.1485 (H)
LCD Type	16.7M Color / Transmissive / Normal Black
TFT Controller IC	ST7703
View Angle	Free
CTP Controller IC	GT9271
CTP Interface	IIC
Weight(g)	TBD
Firmware	TBD
Test Configuration	TBD

5. Dimensional Outline:



6. Electrical Characteristics

6-1 Absolute Maximum Ratings

6-1-1 TFT Absolute Maximum Ratings (Ta=25℃)

Item	Symbol	Min.	Type	Max.	Unit	Remark
Supply Voltage(logic)	IOVDD	-0.3	-	5.5	V	
Supply Voltage(Analog)	VDD	-0.3	-	6.6	V	
Driver supply voltage	VGH-VGL	-0.3	-	+35.0	V	
Operating Temperature	Topr	-20	-	+70	℃	
Storage Temperature	Tstg	-30	-	+80	℃	

Note1: Absolute maximum rating is the limit value beyond which the IC maybe broken. They do not assure operations.

6-1-2 TP Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Analog power AVDD28 (please refer to AGND)	-0.3	3.47	V
VDDIO (please refer to DGND)	-0.3	3.47	V
Voltage on digital I/O	-0.3	3.47	V
Voltage on analog I/O	-0.3	3.47	V
Range of storage temperature	-60	125	℃
ESD susceptibility (HBM)	±4		KV

6-2 Operating Conditions

6-2-1 TFT Operating Conditions (Ta=25℃)

Item	Symbol	Condition	Min.	Type	Max.	Unit	Remark
Power Supply for **logic** Voltage	IOVDD	-	1.65	1.8	2.0	V	
Power supply for **analog** voltage	VDD	-	2.5	2.8	3.3	V	
Supply Voltage	VIH	-	0.7IOVDD	-	IOVDD	V	
	VIL	-	GND	-	0.3IOVDD	V	
	VOH	-	0.8IOVDD	-	IOVDD	mA	
	VOL	-	GND	-	0.2IOVDD	V	
Power Supply Current	IDD	VDD=2.8V	-	TBD	-	mA	

6-2-2 TP Operating Conditions

Parameter	Min.	Typ.	Max.	Unit
AVDD28①	2.7	2.8/3.0/3.3	3.4	V
VDDIO②	-	1.8	-	V
Operating temperature	-20	25	85	℃

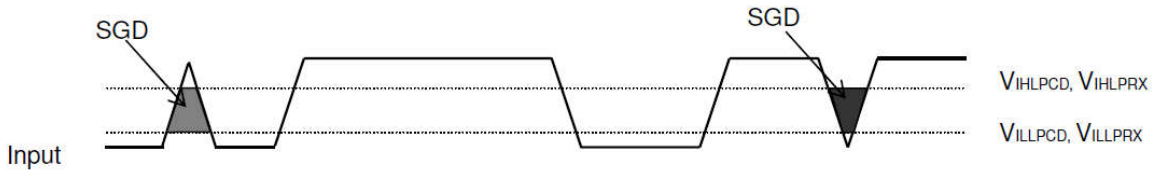
6-3 Timing Characteristics

6-3-1 TFT DSI DC Characteristics

6-3-1-1 LP Mode

LP Mode

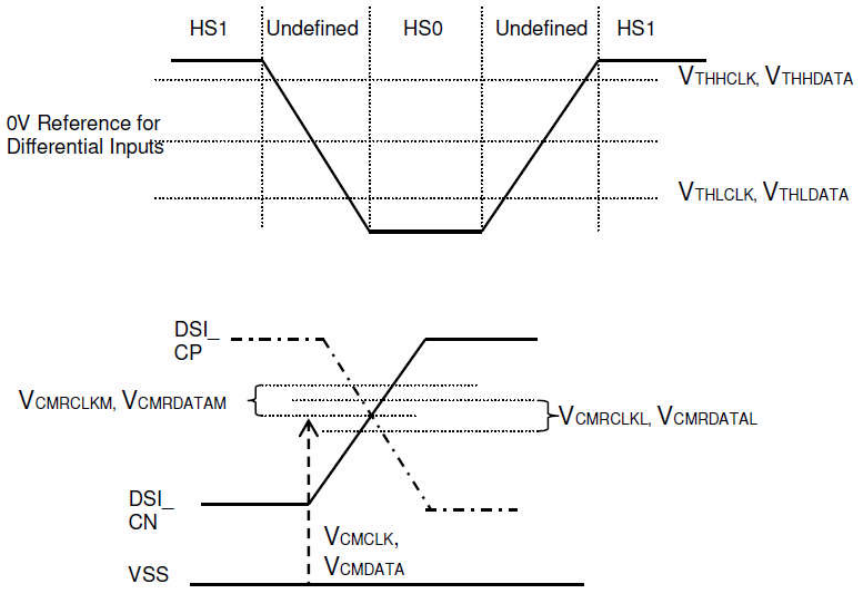
Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level input voltage	V_{ILLPCD}	LP-CD	0	-	200	mV
Logic high level input voltage	V_{IHLPRX}	LP-RX(CLK, D0)	880	-	1350	mV
Logic low level input voltage	V_{ILLPRX}	LP-RX(CLK, D0)	0	-	550	mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX(CLK ULP mode)	0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX(D0)	1.1	-	1.3	V
Logic low level output voltage	V_{OLLPTX}	LP-TX(D0)	-50	-	50	mV
Logic high level input current	V_{IH}	LP-CD, LP-RX	-	-	10	uA
Logic low level input current	V_{IL}	LP-CD, LP-RX	-10	-	-	uA
Input pulse rejection	SGD	DSI-CLK+/-, DSI-D0+/1	-	-	300	Vps



Input glitch rejections of low-power receivers

6-3-1-2 High Speed Mode

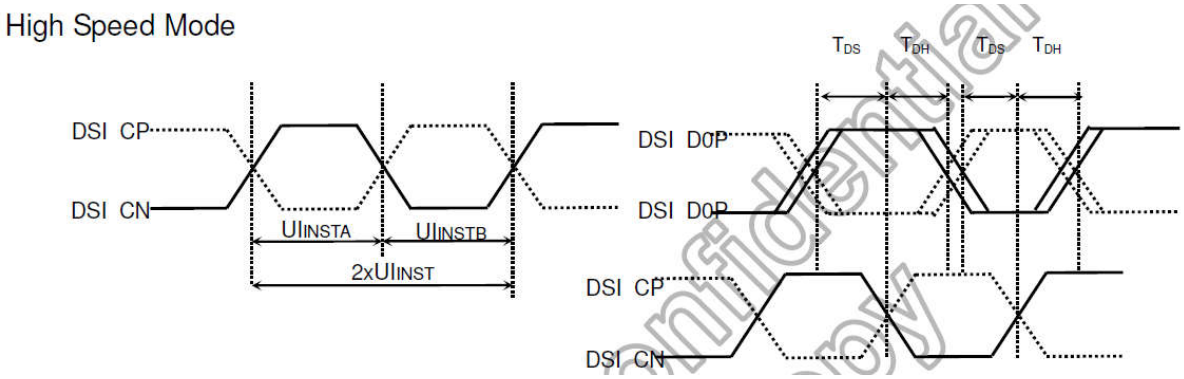
Parameter	Symbol	Conditions	Spec.			Unit
			Min.	Typ.	Max.	
Input common mode	V_{CMCLK} V_{CMDATA}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	70	-	330	mV
Input common mode variation <450 MHZ	$V_{CMRCLKL}$ $V_{CMRDATAL}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-50	-	50	mV
Input common mode variation >450 MHZ	$V_{CMRCLKM}$ $V_{CMRDATAM}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	100	mV
Low-level differential Input threshold	V_{THLCLK} $V_{THLDATA}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-70	-	-	mV
High-level differential Input threshold	V_{THHCLK} $V_{THHDATA}$	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	70	mV
Single ended input low voltage	V_{ILHS}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-40	-	-	mV
Single ended input high voltage	V_{IHHS}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	460	mV
Differential input termination resistor	R_{TERM}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	80	100	125	Ω
Single-ended threshold voltage for termination enable	V_{TERMEN}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	450	mV
Termination capacitor	C_{TERM}	DSI_CP/DSI_CN DSI_D0P/DSI_D0P	-	-	-	pF



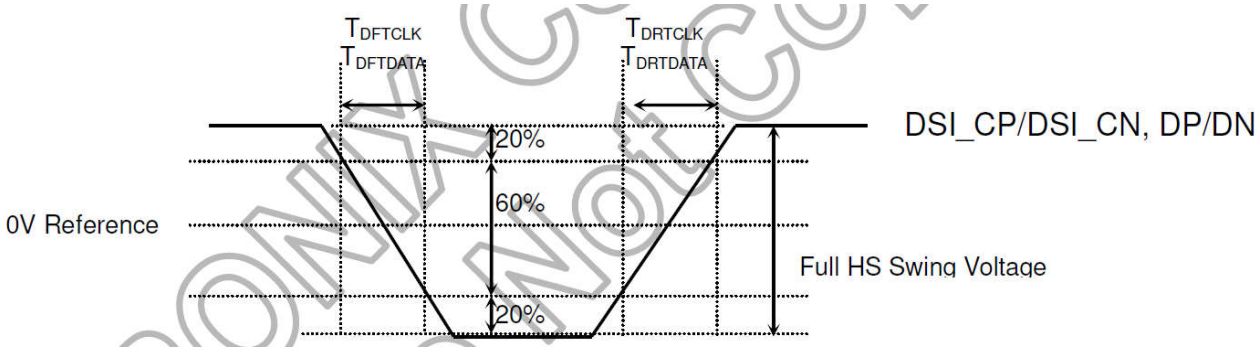
Differential voltage range and command mode voltage

6-3-2 TFT DSI Interface Timing Characteristics

6-3-2-1 High Speed Mode



DSI clock timing characteristics



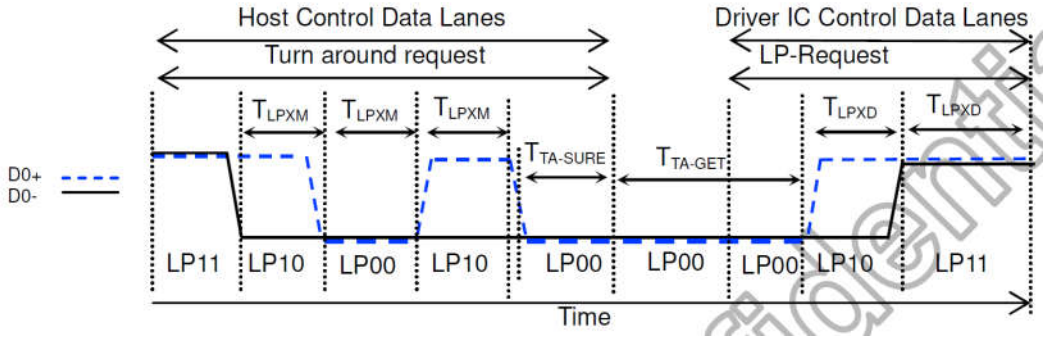
Rising and falling time on clock and data channel

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.5V to 3.3V, T_A = -30 to 70°C)

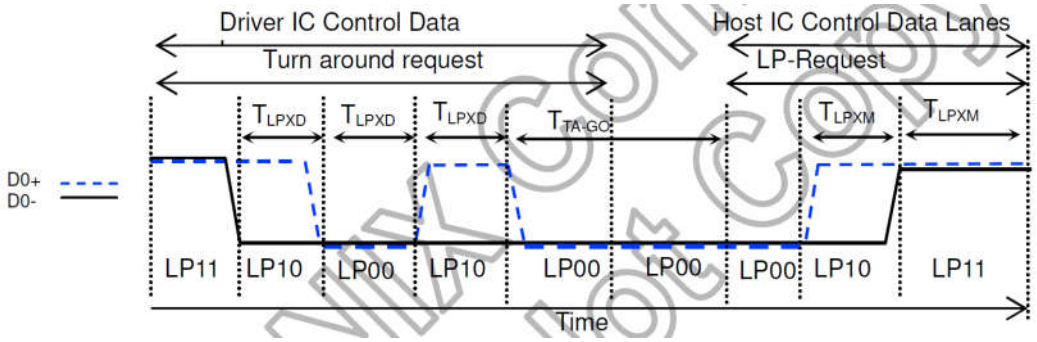
Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Double UI instantaneous	$2xU_{INST}$	TBD	-	25	ns
	UI instantaneous	U_{INSTA} U_{INSTB}	TBD	-	12.5	ns
DP/DN	Data to clock setup time	T_{DS}	0.15xUI	-	-	ps
	Data to clock hold time	T_{DH}	0.15xUI	-	-	ps
DSI_CP/ DSI_CN	Differential rise time for clock	T_{DRTCLK}	150	-	0.3UI	ps
	Differential fall time for clock	T_{DFTCLK}	150	-	0.3UI	ps
DP/DN	Differential rise time for data	$T_{DRTDATA}$	150	-	0.3UI	ps
	Differential fall time for data	$T_{DFTDATA}$	150	-	0.3UI	ps

DSI High speed mode Characteristics

6-3-2-2 Low Speed Mode



BTA from HOST to display module timing



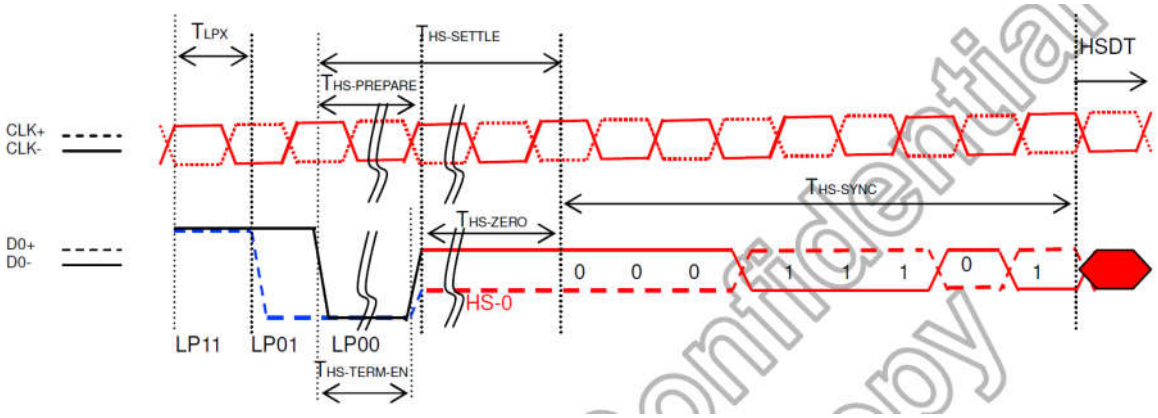
BTA from display module timing to HOST

(VSSA=0V, IOVCC=1.65V to 3.3V, VCI=2.3V to 3.3V, T_A = -30 to 70°C)

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11 Host→ Display module	T_{LPXM}	50	-	-	ns
	Length of LP-00/LP01/LP10/LP11 Display module →Host	T_{LPXD}	50	-	-	ns
	Time-out before the MPU start driver	$T_{TA-SURE}$	T_{LPXD}	-	$2xT_{LPXD}$	ns
	Time to drive LP-00 by display module	T_{TA-GET}	$5xT_{LPXD}$	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	$4xT_{LPXD}$	-	-	ns

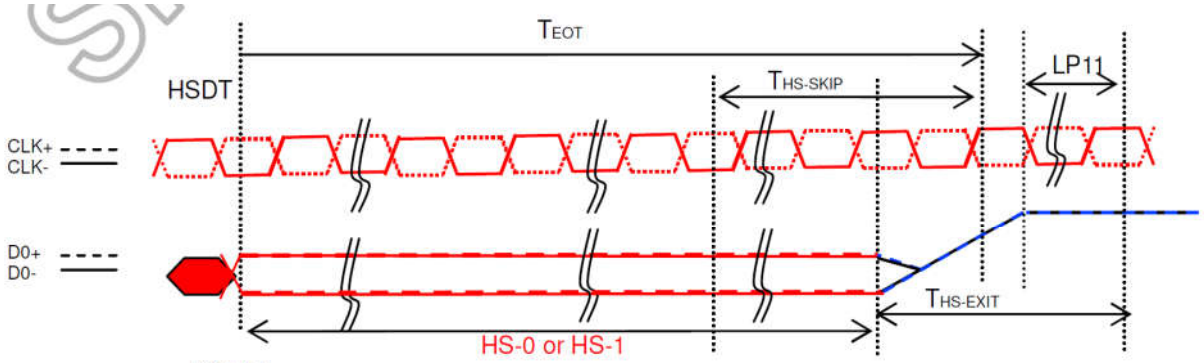
DSI low power mode characteristics

6-3-3 TFT DC bursts Mode



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Length of LP-00/LP01/LP10/LP11	T_{LPX}	50	-	-	ns
	Time to Driver LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI	-	85+6UI	ns
	Time to enable data receiver line termination	$T_{HS-TERM-EN}$	-	-	35+4xUI	ns
	Time to drive LP-00 by display module	T_{TA-GET}	5xT_{LPXD}	-	-	ns
	Time to drive LP-00 after turnaround request Host	T_{TAGO}	4xT_{LPXD}	-	-	ns

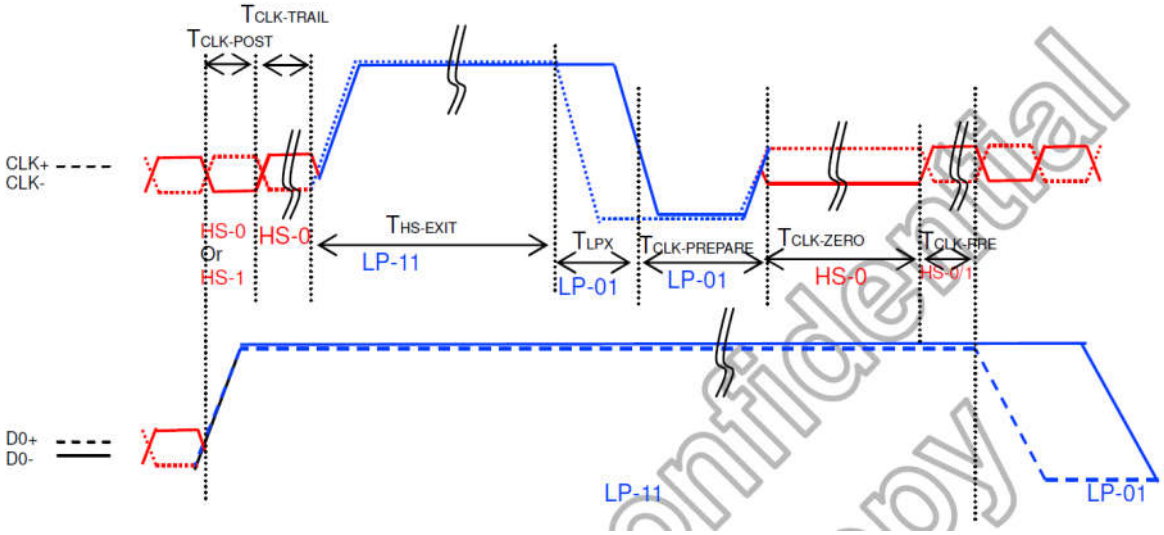
Table 7.5: DSI Low Power Mode to High Speed Mode Timing



NOTE:
If the last bit is HS-0, the transmitter changes from HS-0 to HS-1
If the last bit is HS-0, the transmitter changes from HS-1 to HS-0

Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_D0P/ DSI_D0P	Time-Out at Display Module to Ignore Transition Period of EoT	$T_{HS-SKIP}$	40	-	55+4xUI	ns
	Time to Driver LP-11 after HS Burst	$T_{HS-EXIT}$	100	-	-	ns

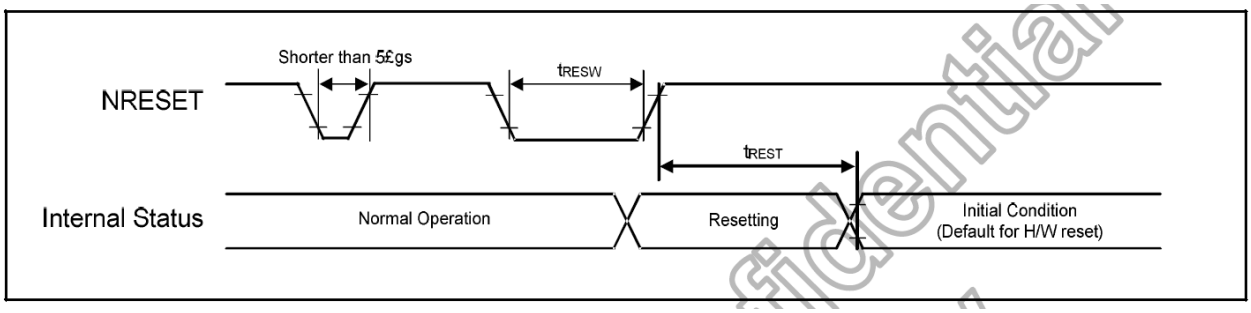
DSI low power mode to high speed mode timing



Signal	Item	Symbol	Spec.			Unit
			Min.	Typ.	Max.	
DSI_CP/ DSI_CN	Time that the MCU shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+52xUI	-	-	ns
	Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	-	-	ns
	Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100	-	-	ns
	Time to drive LP-00 to prepare for HS transmission	$T_{CLK-PREPARE}$	38	-	95	ns
	Time-out at Clock Lane Display Module to enable HS Termination	$T_{CLK-TERM-EN}$	-	-	38	ns
	Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	300	-	-	ns
	Time that the HS clock shall be driven prior to any associated data Lane beginning the transition from LP to HS mode	$T_{CLK-PRE}$	8xUI			

Clock lanes high speed mode to low power mode timing

6-3-4 TFT Reset input Timing



Reset input timing

Symbol	Parameter	Related Pins	Spec.			Note	Unit
			Min.	Typ.	Max.		
tRESW	Reset low pulse width(1)	NRESET	10	-	-	-	µs
tREST	Reset complete time(2)	-	15	-	-	When reset applied during SLPIN mode	ms
		-	120	-	-	When reset applied during SLPOUT mode	ms

Reset input timing

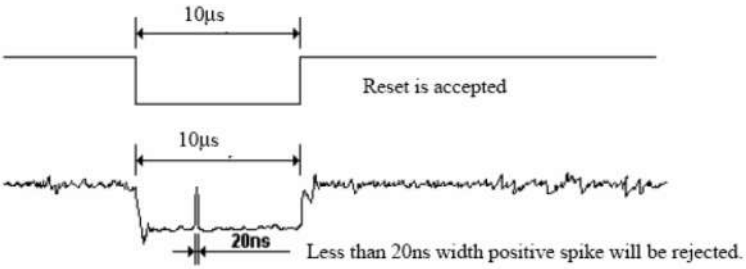
Note:(1)Spike due to an electrostatic discharge on NRESET line does not cause irregular system reset according to the following table

NRESET Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which Maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then return to Default condition for H/W reset.

(3) During Reset Complete Time, ID and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 15ms after a rising edge of NRESET.

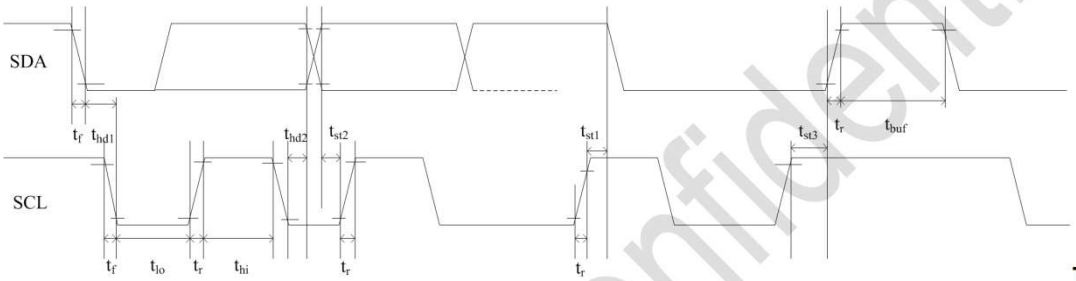
(4) Spike Rejection also applies during a valid reset pulse as shown as below:



(5) It is necessary to wait 15msec after releasing NRESET before sending commands. Also Sleep Out command cannot be sent for 120msec.

6-3-5 TP I2C Tinming

GT9271 provides a standard I2C interface for SCL and SDA to communicate with the host. GT9271 always serves as slave device in the system with all communication being initialized by the host. It is strongly recommended that transmission rate be kept at or below 400Kbps. The I2C timing is shown below:



Test condition 1: 1.8V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for Start condition	t_{st1}	0.6	-	us
SCL setup time for Stop condition	t_{st3}	0.6	-	us
SCL hold time for Start condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	us

Test condition 2: 3.3V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor

Parameter	Symbol	Min.	Max.	Unit
SCL low period	t_{lo}	1.3	-	us
SCL high period	t_{hi}	0.6	-	us
SCL setup time for Start condition	t_{st1}	0.6	-	us
SCL setup time for Stop condition	t_{st3}	0.6	-	us
SCL hold time for Start condition	t_{hd1}	0.6	-	us
SDA setup time	t_{st2}	0.1	-	us
SDA hold time	t_{hd2}	0	-	Us

GT9271 supports two I²C slave addresses: 0xBA/0xBB and 0x28/0x29. The host can select the address by changing the status of Reset and INT pins during the power-on initialization phase. See the diagram below for detailed timings:

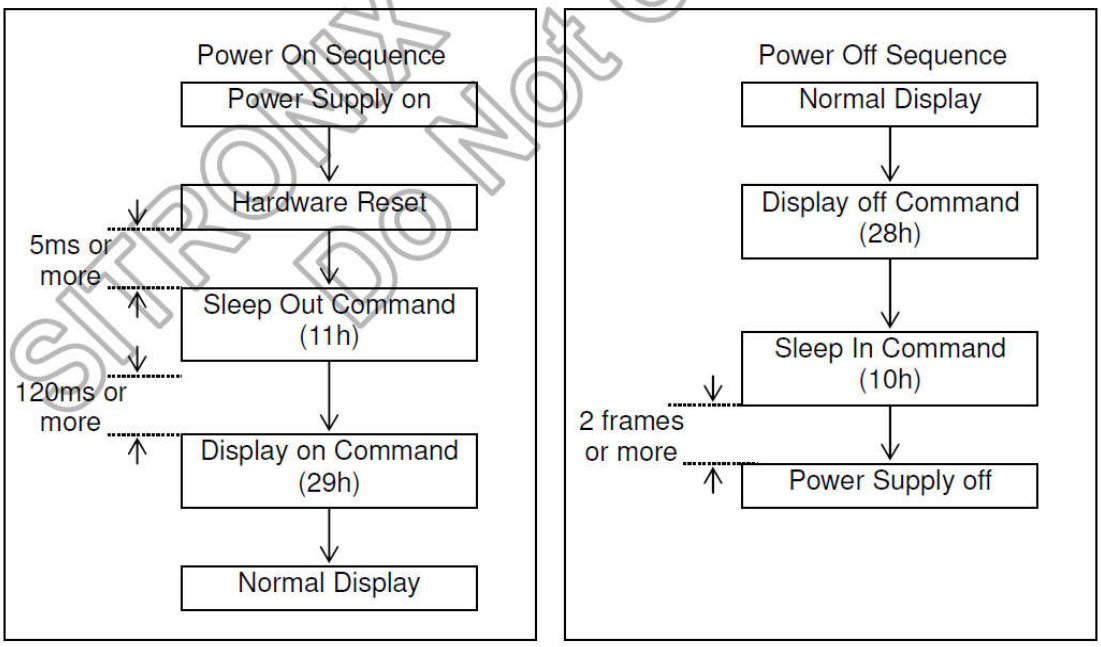
6-3-6 TFT Power ON/OFF Sequence

Power source IOVCC, VCI can be applied and powered down in any order. IOVCC, VCI can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, IOVCC, VCI must be powered down minimum 120msec after NRESET has been released.

During power off, if LCD is in the Sleep In mode, IOVCC, VCI can be powered down minimum 0msec after NRESET has been released.

NCS can be applied at any timing or can be permanently grounded. NRESET has priority over NCS.



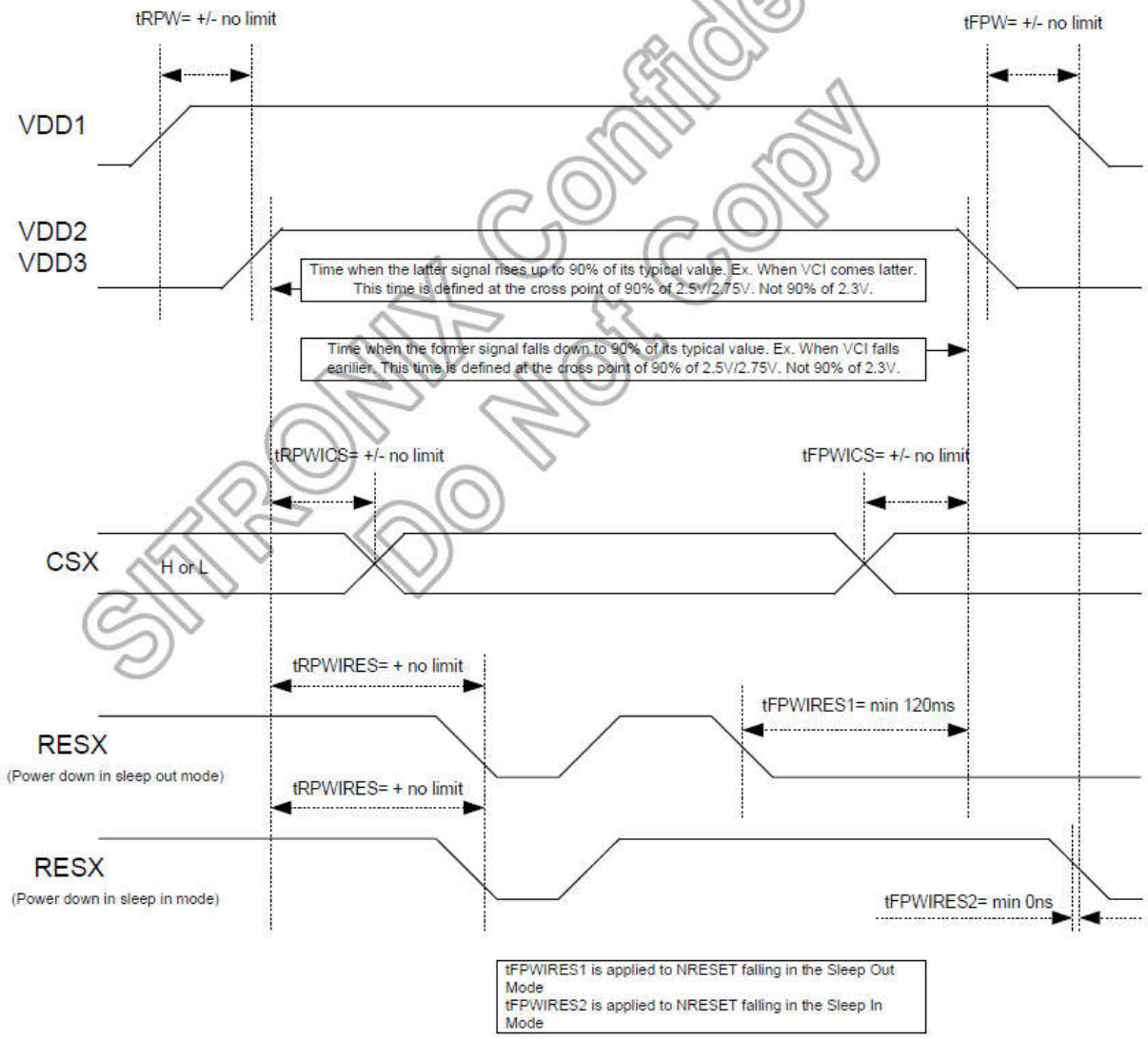
The power supply ON/OFF setting for display ON/OFF and sleep in/out

The uncontrolled power-off means a situation which removed a battery without the controlled power off sequence. It will neither damage the module or the host interface.

If uncontrolled power-off happened, the display will go blank and there will not any visible effect on the display (blank display) and remains blank until “Power On Sequence” powers it up.

6-3-7 RESX line is held high or unstable by host power on

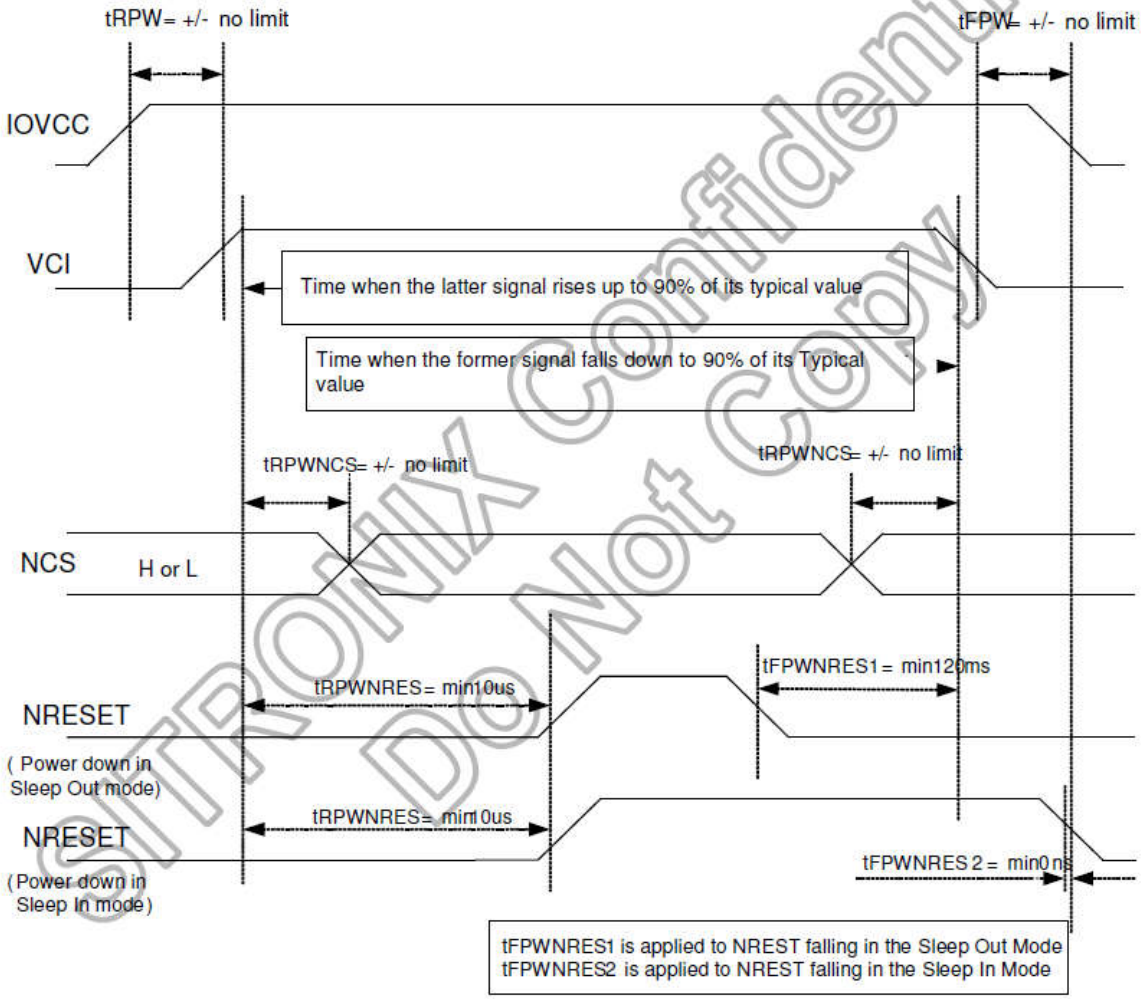
If RESX line is held high or unstable by the host during power on, then a Hardware Reset must be applied after both VDD1, VDD2 and VDD3 have been applied- otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



RESX line is held high or unstable by host at power on

6-3-8 RESX line is held low by host at power on

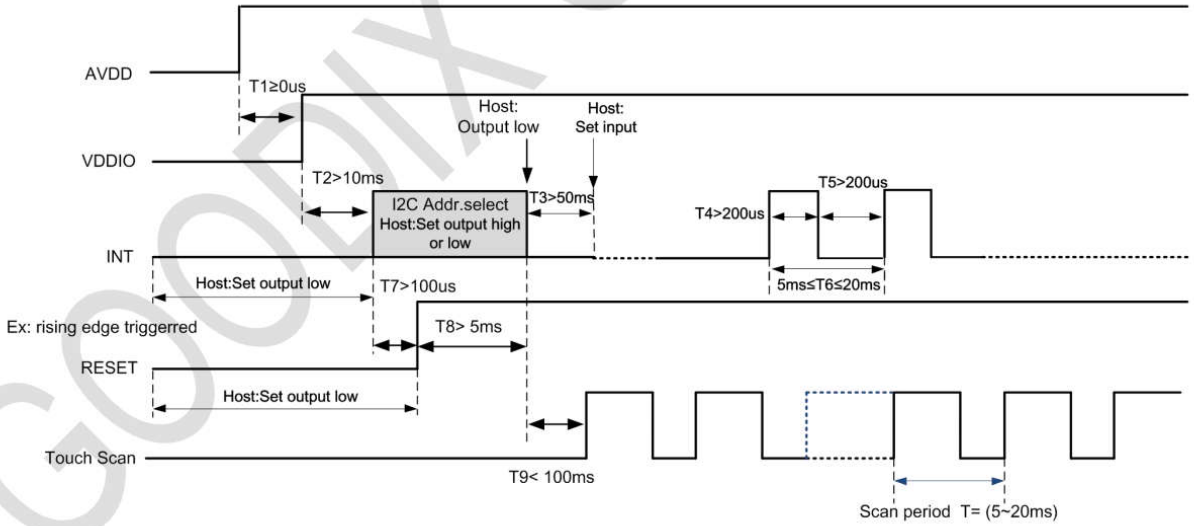
If RESX line is held low (and stable) by the host during power on, then the RESX must be held low for minimum 10µsec after both VDD1, VDD2 and VDD3 have been applied.



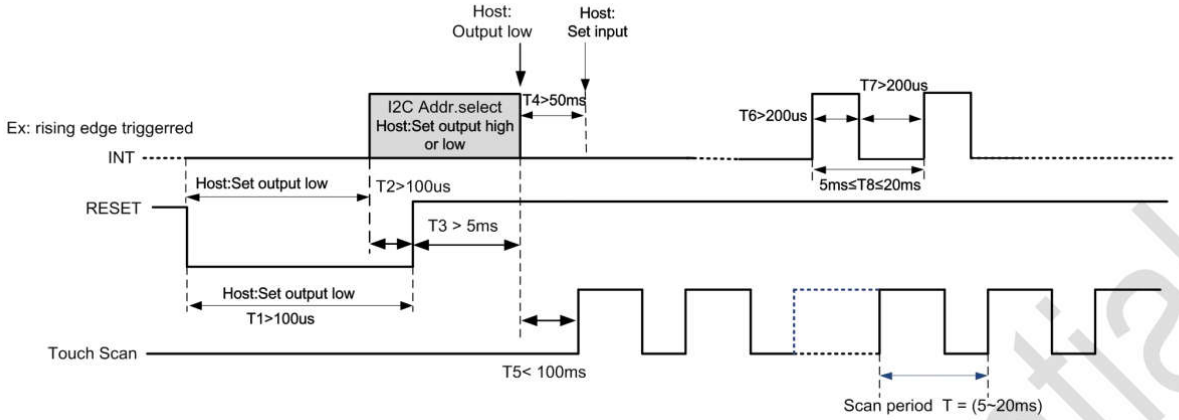
Note: Unless otherwise specified timings herein show cross point at 50% of signal/power level

RESX line held low by host at power on

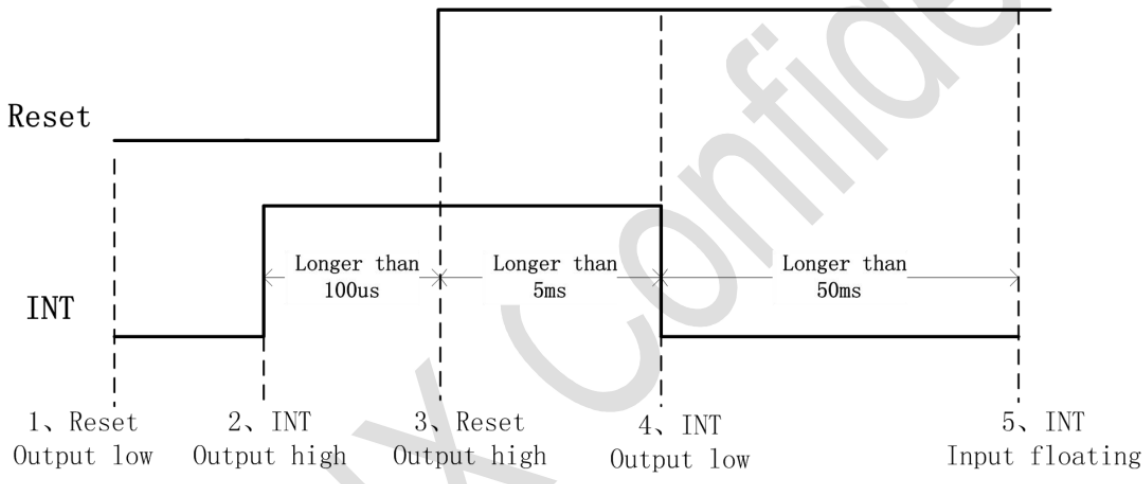
6-3-9 TP Power ON Timing



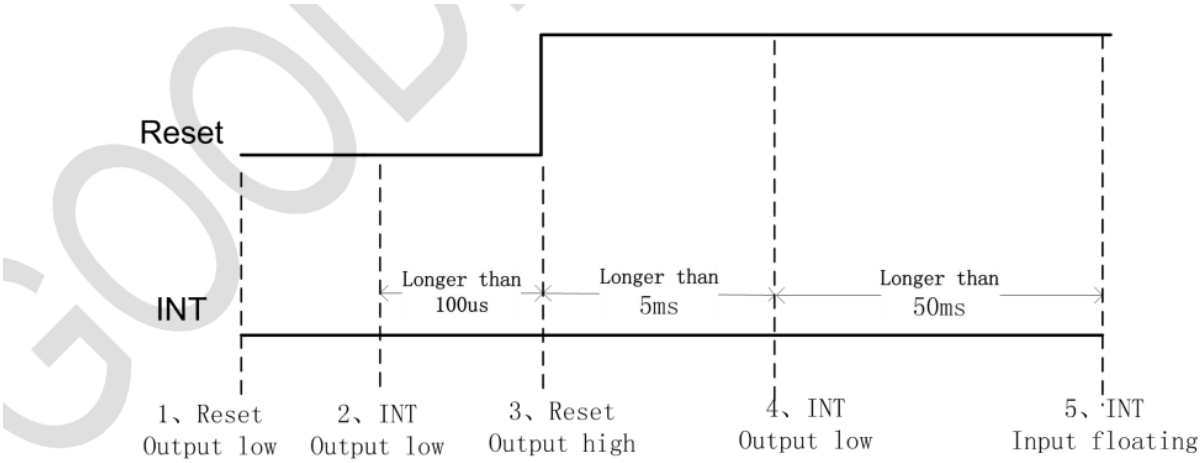
6-3-10 TP Timing for host resetting GT9271



6-3-11 TP Timing for setting slave address to 0x28/0x29



6-3-12 TP Timing for setting slave address to 0xBA/0xBB



7. Optical Characteristics:

Item		Symbol	Conditions	Specifications			Unit	Note
				Min	Typ	Max		
Transmittance		T(%)	-	3.7	4.3	-	-	-
Contrast Ratio		CR	θ=0 Normal Viewing angle	700	900	-		(1) (2)
Response time		TR+TF	-	-	30	35	ms	(1) (3)
NTSC			-	65	70	-	%	
Viewing angle	Hor.	Θx+	CR≧10	70	80	-	deg.	-
		Θx-		70	80	-		
	Ver.	Θy+		70	80	-		
		Θy-		70	80	-		

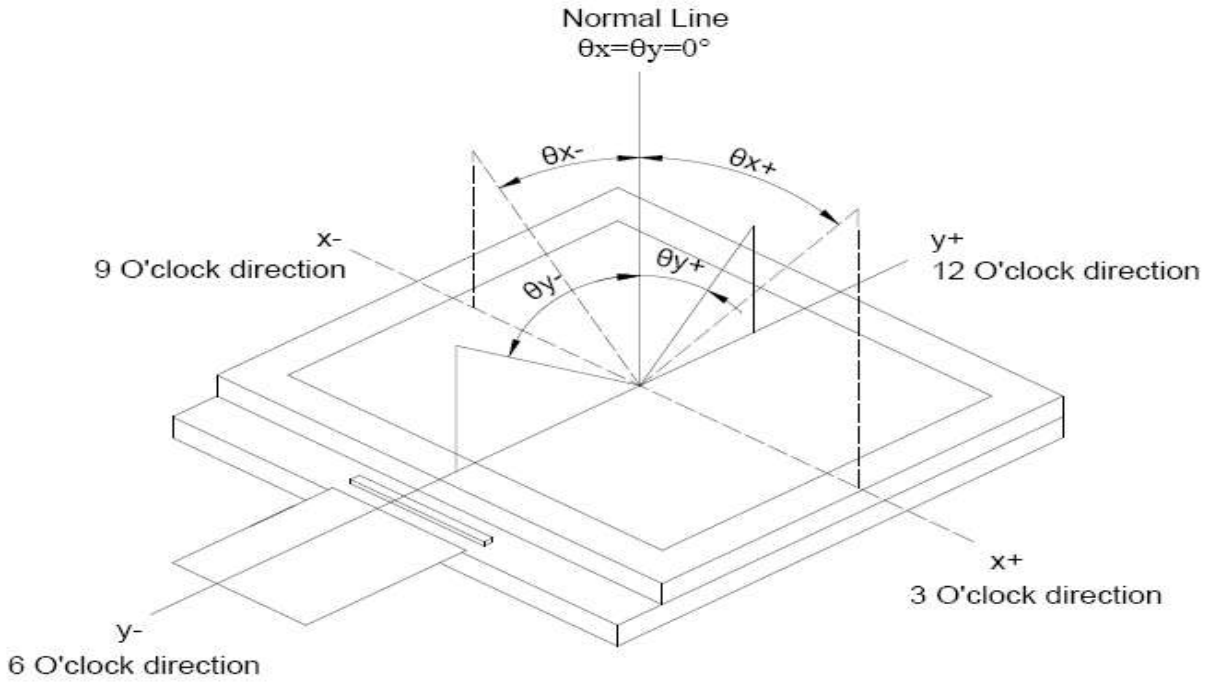
Measuring Condition

1. Measuring surrounding: dark room
2. Ambient temperature: 25±2℃
3. 30 min. Warm-up time.

Color of CIE Coordinate:

Item		Symbol	Condition	Min.	Typ.	Max.
Chromaticity Coordinates (Transmissive)	Red	x	θ = φ = 0° LED Backlight Color Degree	TBD	TBD	TBD
		y		TBD	TBD	TBD
	Green	x		TBD	TBD	TBD
		y		TBD	TBD	TBD
	Blue	x		TBD	TBD	TBD
		y		TBD	TBD	TBD
	White	x		TBD	0.300	TBD
		y		TBD	0.329	TBD

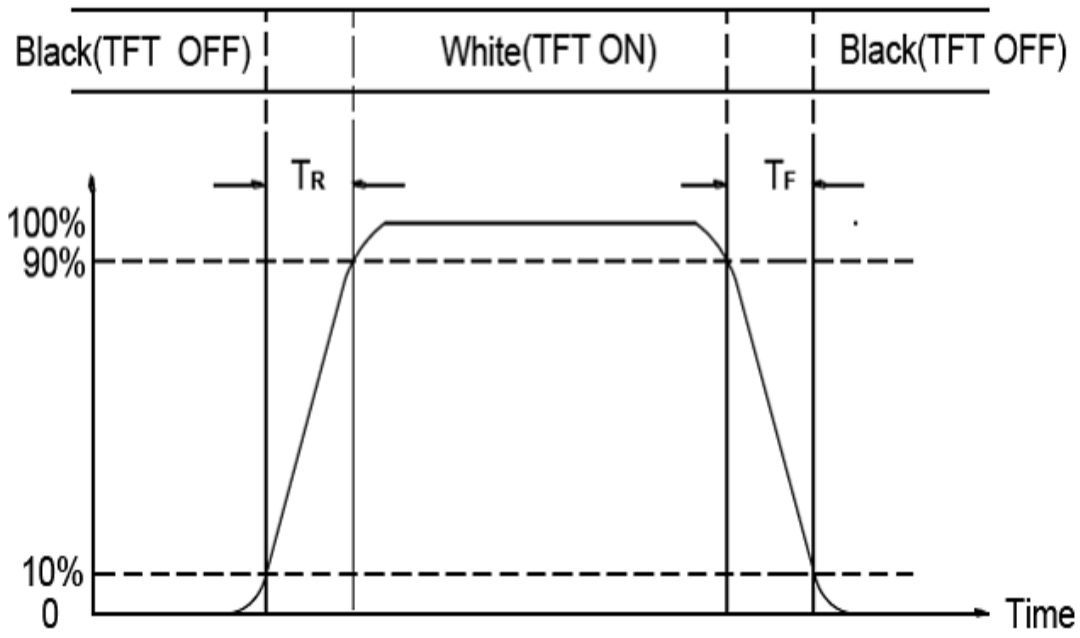
Note (1) Definition of Viewing Angle :



Note (2) Definition of Contrast Ratio(CR) :
measured at the center point of panel

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black}}$$

Note (3) Definition of Response Time : Sum of TR and TF



8. Interface Pin Assignment:

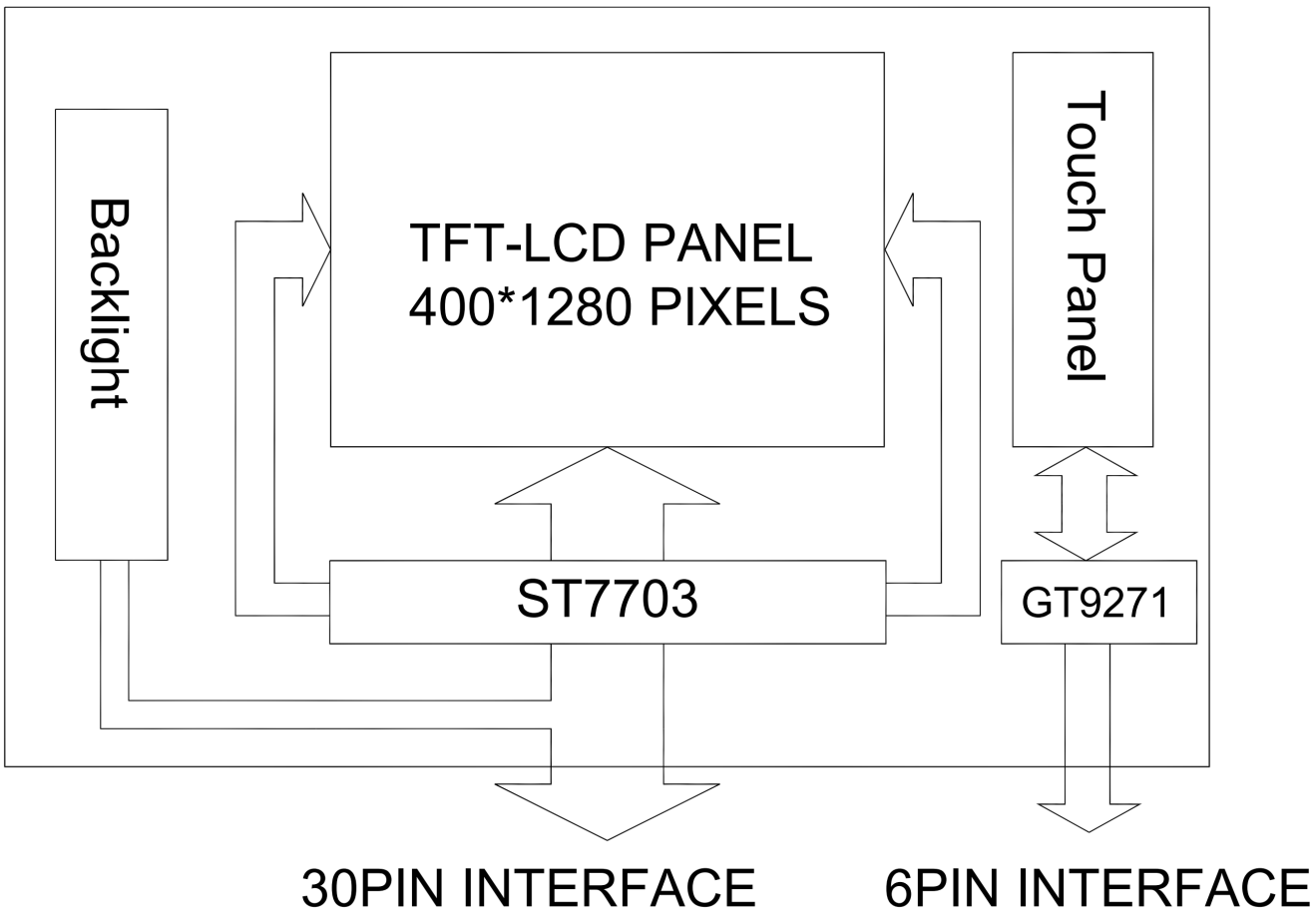
8-1 TFT Pin Assignment

No.	Symbol	Function
1	GND	Ground
2	GND	Ground
3	GND	Ground
4	D0P	MIPI Data lane0 positive input
5	D0N	MIPI Data lane0 negative input
6	GND	Ground
7	D1P	MIPI Data lane1 positive input
8	D1N	MIPI Data lane1 negative input
9	GND	Ground
10	CLKP	MIPI clock positive input
11	CLKN	MIPI clock negative input
12	GND	Ground
13	D2P	MIPI Data lane2 positive input
14	D2N	MIPI Data lane2 negative input
15	GND	Ground
16	D3P	MIPI Data lane3 positive input
17	D3N	MIPI Data lane3 negative input
18	GND	Ground
19	GND	Ground
20	RESET	Global reset pin
21	GND	Ground
22	VDDI	Power supply to the internal logic
23	VDD	Power supply to the internal Analog
24	GND	Ground
25	GND	Ground
26	LEDA	Power supply Anode input for backlight
27	LEDK	Power supply Cathode input for backlight
28	GND	Ground
29	GND	Ground
30	GND	Ground

8-2 TP Pin Assignment

No.	Name	Function Description
1	GND	Ground
2	SCL	I²C clock signal
3	SDA	I²C data signal
4	INT	Interrupt signal
5	RESET	Reset pin
6	VDD 3.3V	Analog power

9. Block Diagram:



10. Backlight:

1. Standard Lamp Styles (Edge Lighting Type):
   The LED chips are distributed over the edge light area of the illumination unit, which gives the less power consumption:

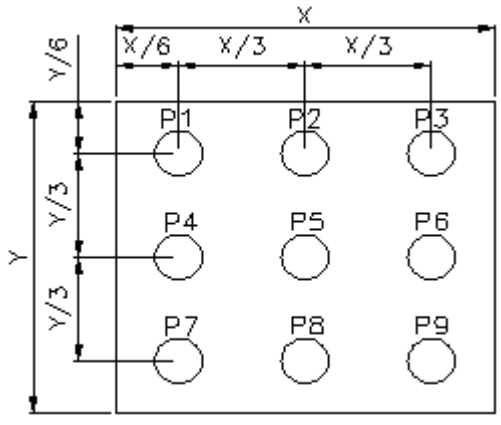
2. The Main Advantages of the LED Backlight are as following:
   2.1 The brightness of the backlight can simply be adjusted.
   By a resistor or a potentiometer.

3. Data About LED Backlight: (Ta=25°)

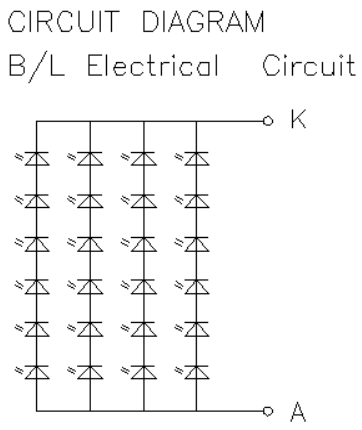
PARAMETER	Sym.	Min.	Typ.	Max.	Unit	Test Condition	Note
Supply Current	I	-	160	-	mA	V=18.6V	
Supply Voltage	V	16.2	18.6	21.0	V	If=160mA	1
Luminous Intensity for LCM (Without TP)	IV	340	380	-	Cd/m2		2
Uniformity for LCM	-	70	-	-	%		3
Life Time	-	20000	-	-	Hr.		4
Color	White						

NOTE:
1. Backlight Only
2. Average Luminous Intensity of P1-P9
3. Uniformity = Min/Max * 100%
4. LED life time defined as follow: the final brightness is at 50% of original brightness

Measured Method: (X*Y: Light Area)



Internal Circuit Diagram



Using aperture of 1°, distance 50cm.

11. Standard Specification for Reliability :

11–1. Standard Specifications for Reliability

No	Item	Description
01	High temperature operation	The sample should be allowed to stand at 70℃ for 240 hours under driving condition and then returning it to normal temperature condition, and allowing it stand for 2 hours.
02	Low temperature operation	The sample should be allowed to stand at -20℃ for 240 hours under driving condition and then returning it to normal temperature condition, and allowing it stand for 2 hours.
03	High temperature storage	The sample should be allowed to stand at 80℃ for 240 hours under no-load condition, and then returning it to normal temperature condition, and allowing it stand for 2 hours.
04	Low temperature storage	The sample should be allowed to stand at -30℃ for 240 hours under no-load condition, then returning it to normal temperature condition, and allowing it stand for 2 hours.
05	Moisture storage	The sample should be allowed to stand at 60℃,90%RH MAX for 240 hours under no-load condition, then taking it out and drying it at normal temperature for 2 hours.
06	Thermal shock storage	The sample should be allowed to stand the following 10 cycles : -30℃ for 30 minutes → normal temperature for 5 minutes → +80℃ for 30 minutes → normal temperature for 5 minutes, as one cycle.
07	Packing vibration	Frequency range : 10Hz ~ 55Hz Amplitude of vibration : 1.5mm Sweep time: 12 min X,Y,Z 2 hours for each direction.
08	Packing drop test	According to ISTA 1A 2001.
09	Electrical Static Discharge	Air: ±6KV 150pF/330Ω 5 times
		Contact: ±4KV 150pF/330Ω 5 time

*Sample size for each test item is 3~5pcs

11 - 2. Testing Conditions and Inspection Criteria

For the final test the testing sample must be stored at room temperature for 24 hours, after the tests listed in Table 11-1, Standard specifications for Reliability have been executed in order to ensure stability.

No	Item	Test Model	In section Criteria
01	Current Consumption	Refer To Specification	The current consumption should conform to the product specification.
02	Contrast	Refer To Specification	After the tests have been executed, the contrast must be larger than half of its initial value prior to the tests.
03	Appearance	Visual inspection	Defect free.

11- 3. MTBF

MTBF	Functions, performance, appearance, etc. shall be free from remarkable deterioration within 50,000 hours under ordinary operating and storage conditions room temperature (25±5℃), normal humidity (50±10% RH), and in area not exposed to direct sun light.

12. Specification of Quality Assurance:

12-1. Purpose

This standard for Quality Assurance should affirm the quality of LCD module products to supply to purchaser by YEEBO CORPORATION (Supplier).

12-2. Standard for Quality Test

a. Inspection:

Before delivering, the supplier should take the following tests, and affirm the quality of product.

b. Electro-Optical Characteristics:

According to the individual specification to test the product.

c. Test of Appearance Characteristics:

According to the individual specification to test the product.

d. Test of Reliability Characteristics:

According to the definition of reliability on the specification for testing products.

e. Delivery Test:

Before delivering, the supplier should take the delivery test.

(i) Test method: According to **ISO2859-1.**General Inspection Level Ⅱ take a single time.

(ii) The defects classify of AQL as following:

Major defect: AQL = 0.65

Minor defect: AQL = 2.5

Total defects: AQL = 2.5

12-3. Non- conforming Analysis & Deal With Manners

a. Non- conforming Analysis:

(i) Purchaser should supply the detail data of non- conforming sample and the non-conforming.

(ii) After accepting the detail data from purchaser, the analysis of non- conforming should be finished in two weeks.

(iii) If supplier can not finish analysis on time, must announce purchaser before 3 days.

b. Disposition of non- conforming:

(i) If find any product defect of supplier during assembly time, supplier must change the good product for every defect after recognition.

(ii) Both supplier and customer should analyze the reason and discuss the disposition of non- conforming when the reason of nonconforming is not sure.

12-4. Agreement items

Both sides should discuss together when the following problems happen.

a. There is any problem of standard of quality assurance, and both sides should think that must be modified.

b. There is any argument item which does not record in the standard of quality assurance.

c. Any other special problem.

12-5. Standard of The Product Appearance Test

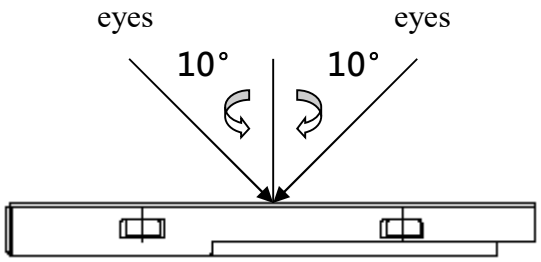
a. Manner of appearance test:

(i) The test must be under 20W × 2 or 40W fluorescent light, and the distance of view must be at 30±5cm.

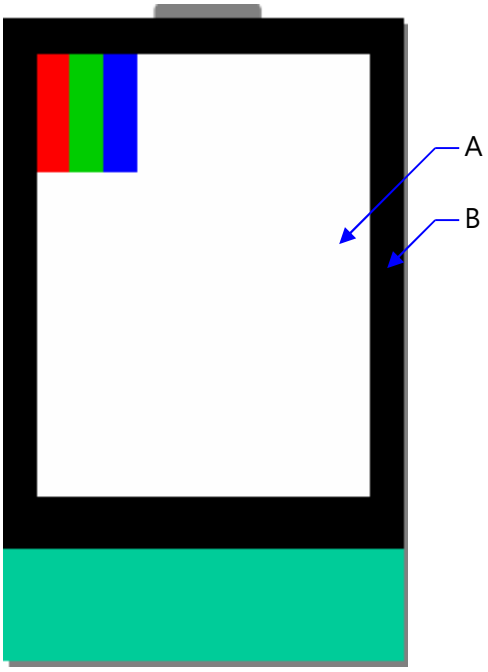
(ii) When test the model of transmissive product must add the reflective plate.

(iii)The test direction is base on around 10° of vertical line.

(iiii)Temperature: 25±5℃ Humidity: 60±10%RH



(iv) Definition of area:



A. Area: Viewing area.

B. Area: Out of viewing area.
(Outside viewing area)

b. Basic principle:

(i) It will accord to the AQL when the standard can not be described.

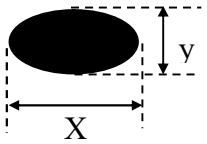
(ii) The sample of the lowest acceptable quality level must be discussed by both supplier and customer when any dispute happened.

(iii) Must add new item on time when it is necessary.

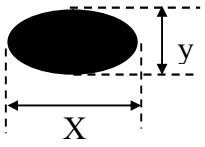
c. Standard of inspection: (Unit: mm)

12-6. Inspection specification

Defect out of viewing area can be neglected.

<table>
<tr><th>Item</th><th>Specification Unit : mm</th><th>AQL</th></tr>
<tr><td>Electrical Testing</td><td>1.1 Open
1.2 Short
1.3 T/P failure
1.4 Missing vertical, horizontal segment, segment contrast defect.
1.5 Missing character, dot or icon.
1.6 Display malfunction.
1.7 No function or no display.
1.8 Current consumption exceeds product specifications.
1.9 LCD viewing angle defect.
1.10 Mixed product types.
1.11 Flicker</td><td>0.65</td></tr>
<tr><td>explosion-proof film bubble/Concave and convex point/indentation / Contamination</td><td>
<table>
<tr><th>D</th><th>Acceptable numbers</th></tr>
<tr><td>≤0.3</td><td>ignored (No more than five spots within 5mm G)</td></tr>
<tr><td>0.3≤D≤0.5</td><td>4</td></tr>
<tr><td>0.5<D≤1.0</td><td>2</td></tr>
<tr><td>1.0<D≤1.5</td><td>2</td></tr>
<tr><td>D>1.5</td><td>NG</td></tr>
</table>


D=(x+y)/2
1、 Product’s front side checked according to this specification, back side ignored, but light leakage is not allowed.
2、 Printing ink peel off is not allowed.
3、 The particle will be ignored when it is removable by cleaning
* Densely spaced: No more than two spots within 10mm</td><td>2.5</td></tr>
</table>

<table>
<tr>
<td>Black spots / White spots /Bright spots/ Color spots /polluted inside/ punctured</td>
<td>
<table>
<tr><th>D</th><th>Acceptable numbers</th></tr>
<tr><td>≤0.2</td><td>ignored (No more than five spots within 5mm)</td></tr>
<tr><td>0.2≤D≤0.4</td><td>4</td></tr>
<tr><td>0.4<D≤0.8</td><td>3</td></tr>
</table>


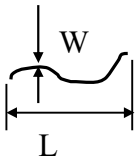
D=(x+y)/2

1、Product’s front side checked according to this specification, back side ignored, but light leakage is not allowed.

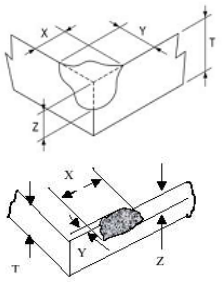
2、Printing ink peel off is not allowed.

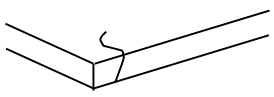
3、The particle will be ignored when it is removable by cleaning

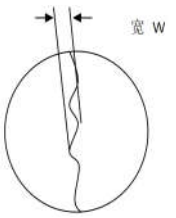
4、Not visible through 5% ND filter

* Densely spaced: No more than two spots within 10mm
</td>
<td>2.5</td>
</tr>
<tr>
<td>Linear Object: Fiber, scurf, scratches and other linear defects (not affecting function)</td>
<td>
<table>
<tr><th>W</th><th>L</th><th>Acceptable numbers</th></tr>
<tr><td>≤0.05</td><td>≤8</td><td>ignored No more than five lines within 5mm)</td></tr>
<tr><td>0.1<W≤0.3</td><td>≤8</td><td>2</td></tr>
<tr><td>W〉0.3</td><td></td><td>NG</td></tr>
</table>


The reverse side scratches, not affect to the electronic circuit, cannot find the scratches from the front side is acceptable

* Densely spaced: No more than two lines within 10mm
</td>
<td>2.5</td>
</tr>
<tr>
<td>Glass edge chipping、edge breakage</td>
<td>
<table>
<tr><td colspan="2">Edge breakage can’t affect visual effection (edge breakage can’t cause damage to circuit); over lens have no visual damage</td></tr>
<tr><td>conditions</td><td>Acceptable numbers</td></tr>
<tr><td>X≤3mm,Y≤2mm, Z≤T</td><td>5</td></tr>
</table>


</td>
<td>2.5</td>
</tr>
<tr>
<td>Glass broken</td>
<td>Visual broken is NG, and there is no potential fault.

</td>
<td>0.65</td>
</tr>
</table>

<table>
<tr><td colspan="2">1. V/A printed edges sawtooth inspected according to this standard
2. LOGO’s sawtooth</td><td>Some contentious defect judged according to samples
<table><tr><td>Product type</td><td>Conditions</td></tr><tr><td>Same size</td><td>1、width below 0.2 inch（included）ignored，above 0.2 NG
2、Length not accounted</td></tr></table></td><td> 
</td><td>2.5</td></tr>
<tr><td colspan="2">Specific dimension</td><td>In accordance with product outline drawing or specification (key dimension) or engineering sample.</td><td></td><td>2.5</td></tr>
<tr><td colspan="2">Glue overflow/Frame</td><td>1. Glue overflow exceed 0.2mm to the black frame is not allowed.
  </td><td></td><td>2.5</td></tr>
<tr><td rowspan="3">FPC</td><td>Bonding bubble/ Misalignment</td><td>FPC golden finger hot pressure’s bubble or impurity diameter shall be below 1/2 of the pressed area, pressed deviation shall not exceed 1/2 of the silver line width, and 40X microscope cannot have obvious cracks.</td><td></td><td>0.65</td></tr>
<tr><td>Folded mark（minor fault）</td><td>Linearity irreversibility folded mark and acute angle folded mark is NG.</td><td></td><td>2.5</td></tr>
<tr><td>EMI FILM（minor fault）</td><td>Surface broken, scratched≦0.3mm
Surface broken below 5mm can be modified by print ink, after modified, the result shall be achieved to EMI</td><td></td><td>2.5</td></tr>
</table>

13. Handling Precaution:

13-1 Handling of LCM

- Don't give external shock.
- Don't apply excessive force on the surface.
- Liquid in LCD is hazardous substance. Must not lick and swallow. when the liquid is attach to your hand, skin, cloth etc. Wash it out thoroughly and immediately.
- Don't operate it above the absolute maximum rating.
- Don't disassemble the LCM.
- The operators should be grounded whenever he/she comes into contact with the module. Never touch any of the conductive parts such as the LSI pads,the copper leads on the PCB and the interface terminals with any parts of the human body.
- The modules should be kept in antistatic bags or other containers resistant to static for storage.
- The module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

13-2 Storage

- Store in an ambient temperature of 25±10℃, and in a relative humidity of 50±10%RH. Don't expose to sunlight or fluorescent light.
- Storage in a clean environment, free from dust, active gas, and solvent.
- Store in anti-static electricity container.
- Store without any physical load.

13-3 Soldering

- Use only soldering irons with proper grounding and no leakage.
- Iron: No higher than 310±10℃ and less than 3 sec during Hand soldering.
- Rewiring: no more than 2 times.

14. Warranty

This product has been manufactured to specifications as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we will not take responsibility if the product is used in medical devices, nuclear power control equipment, aerospace equipment, fire and security systems, or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required. If the product is to be used in any of the above applications, we will need to enter into a separate product liability agreement.

1. We cannot accept responsibility for any defect arise after additional process of the product (including disassembly and reassembly), after product delivery.
2. We cannot accept responsibility for any defect, which may arise after the application of strong external force to the product.
3. We cannot accept responsibility for any defect, which may arise due to the application of static electricity after the product has passed your company's acceptance inspection procedures.
4. We can not accept responsibility for industrial property, which may arise through the use of your product , with exception to those issues relating directly to the structure or method of manufacturing of our product within one year from YEEBO shipment.
5. For Heatseal Product which required to heatseal by customer side, parts must be used within three months after delivery from factory.
6. For TAB Product which required to solder by customer side, parts must be used within three months after delivery from factory.
7. The liability of YB is limited to repair or replacement on the terms set forth below. YB will not be responsible for any subsequent or consequential events or injury or damage to any personnel or user including third party personnel and/or user. Unless otherwise agreed in writing between YB and the customer, YB will only replace or repair any of its LCD which is found defective electrically or visually when inspected in accordance with YB GENERAL LCD INSPECTION STANDARD.

15. Guarantee:

Our products meet requirements of the environment.
YEEBO ROHS requirement is based on European Union Directive 2011/65/EU(ROHS) Requirements and Update.