億 都 集 團
YEEBO GROUP

SPECIFICATION
FOR
LCD MODULE

MODULE NO: YB-TG720720S02A-N-A0

Doc.Version:00

Customer Approval:

□ Accept	□ Reject

YEEBO	NAME	SIGNATURE	DATE
Prepare	Electronic Engineer	伍珏琛	2022-10-14
Check	Mechanical Engineer		2022-10-14
Verify			2022-10-14
Approval			2022-10-14

■ APPROVAL FOR SPECIFICATIONS ONLY

□ APPROVAL FOR SPECIFICATIONS AND SAMPLE

WIMRD005-02-D

Add: 7/F.,On Dak Industrial Building,2-6 Wah Sing Street, Kwai Chung,H.K.
Tel: +852-2945-6800 ; +852-2945-6885
Fax: +852-2481-0019

1. Revision History

Sample Version	DOC. Version	DATE	DESCRIPTION		CHANGED BY
A0	00	2022-10-14	SPEC ONLY	First issue	W.J.C/D.M.G

2. Table of Contents:

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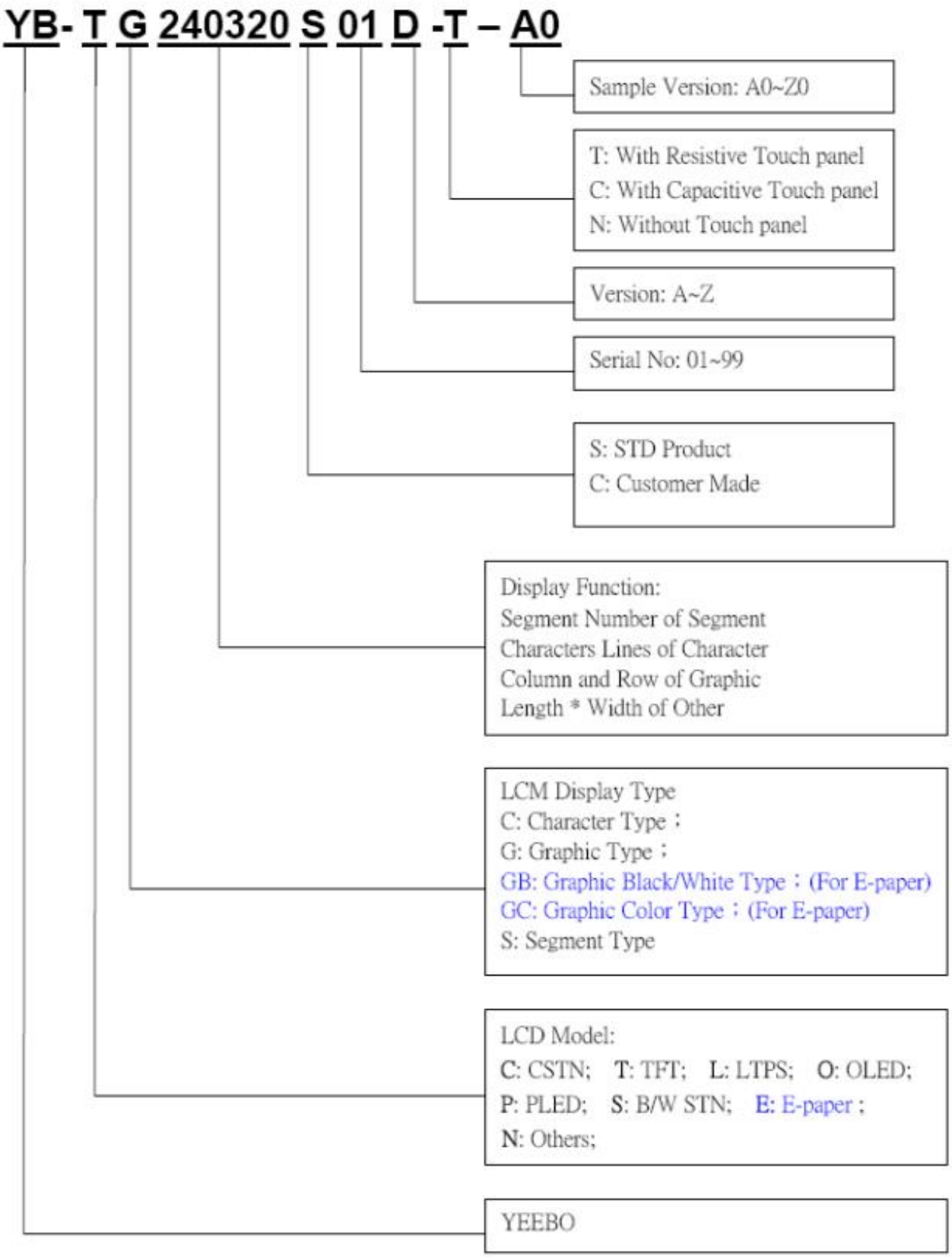
3. Module Numbering System:

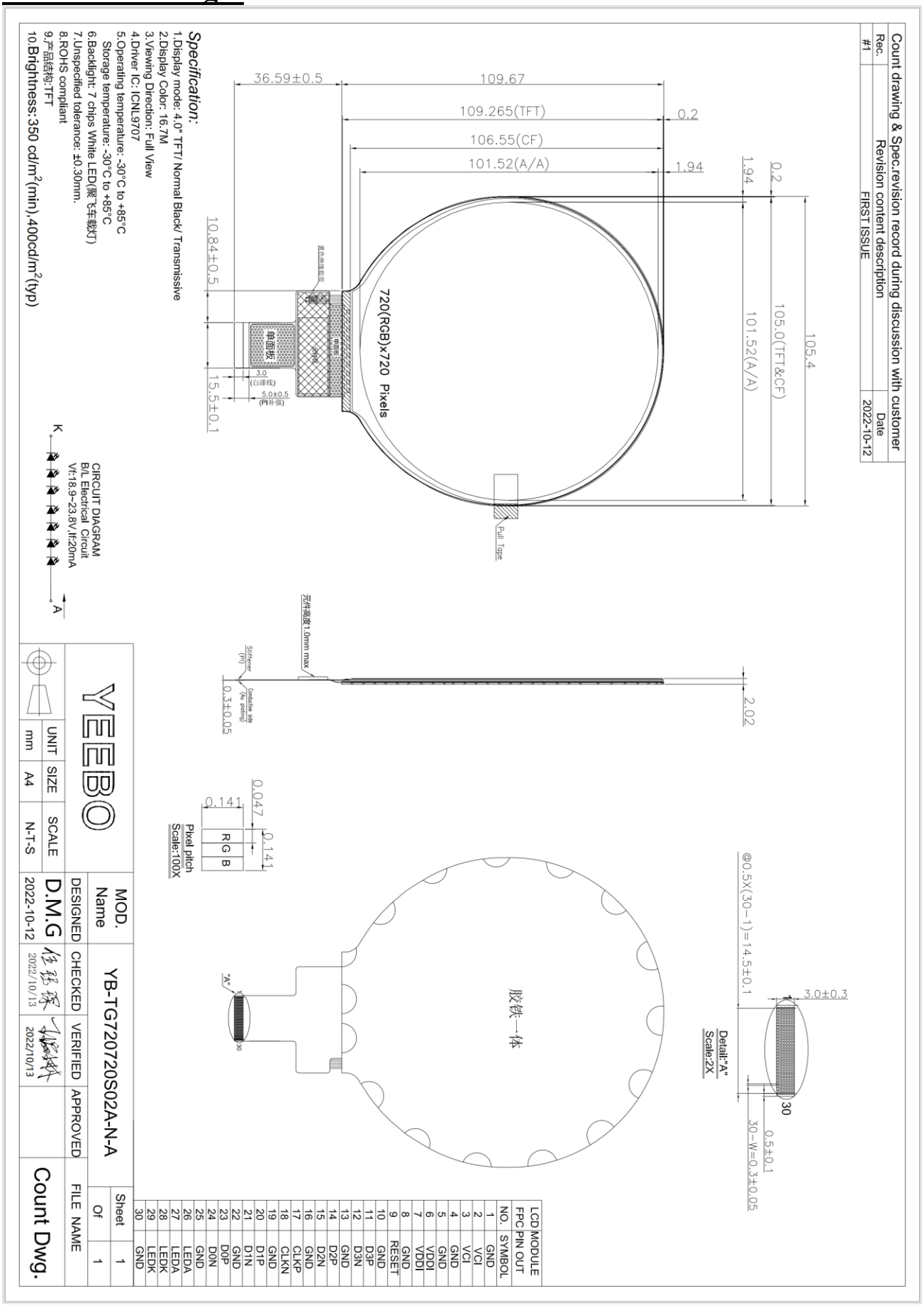
(Example)



4. General Specification:

ITEM	CONTENTS
Module Size	105.4 (W) * 109.67 (H) * 2.02 (T) mm
Module Size (with FPC)	105.4 (W) * 146.26 (H) * 2.02 (T) mm
Display Size (Diagonal)	4.0 inch
Display Format	720(RGB)*720 Pixels
Active Area	101.52(H) ×101.52(V)
Pixel Pitch	0.141(H) mm*0.141 (V) mm
LCD Type	TFT (16.7M)/ Transmissive / NB
The Best Viewing Direction	FREE
Controller IC	ICNL9707
Weight	TBD

5. LCM drawing:



6. Electrical Characteristics

6-1 Absolute Maximum Ratings (Ta=25℃ VSS=0V)

Item	Symbol	Min.	Type	Max.	Unit	Remark
Power Supply Voltage	V_{CI}	-0.3	-	6.6	V	
Operating Temperature	Topr	-30	-	+85	℃	
Storage Temperature	Tstg	-30	-	+85	℃	

Note1: Absolute maximum rating is the limit value beyond which the IC maybe broken. They do not assure operations.

6-2 Operating Conditions (Ta=25℃)

Item	Symbol	Condition	Min.	Type	Max.	Unit	Remark
Power Supply Voltage	V_{CI}	-	2.6	3.0	3.6	V	
	IOVCC		1.65	1.8	1.95	V	
IO Supply Voltage	V_{IH}	-	0.7 IOVCC	-	IOVCC	V	
	V_{IL}	-	V_{SS}	-	0.3 IOVCC	V	
	V_{OH}	-	0.8 IOVCC	-	IOVCC	V	
	V_{OL}	-	V_{SS}	-	0.2 IOVCC	V	
Power Supply Current	I_{DD}	V_{CI}=3.0V	-	TBD	-	mA	

.

6-3 AC Characteristics

High Speed Mode - Clock / Data Timings

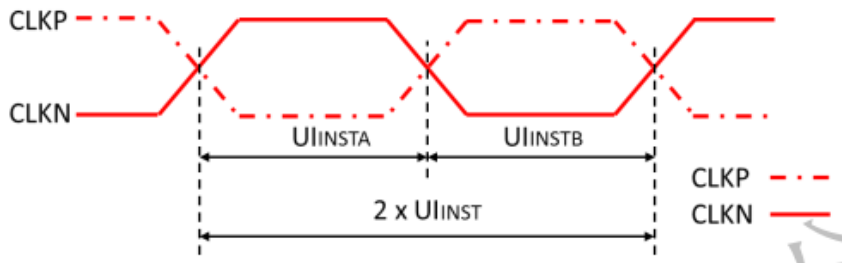


Figure 4-5 Clock Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
CLK P/N	2xUIINST	Double UI instantaneous	2.5		12.5	ns	
CLK P/N	UIINSTA, UIINSTB	UI instantaneous Half	1.25		6.25	ns	1,2

***Note** 1*: UI = UIINSTA = UIINSTB.

***Note** 2*: ICNL9707 can support max 600Mbps/lane at 4 lane and max 800Mbps/lane at 3 lane application.

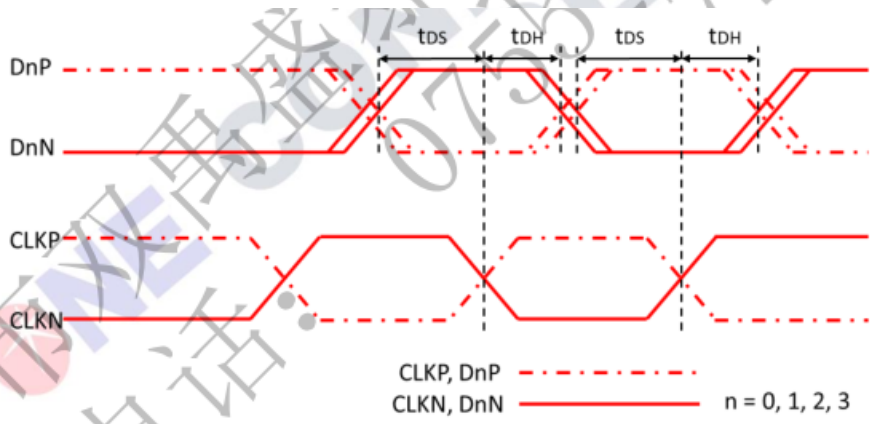


Figure 4-6 DSI Clock / Data Timings

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
Dn P/N (n=0,1,2 and 3)	tDS	Data to Clock Setup time	0.15*UI			UI	
	tDH	Clock to Data Hold time	0.15*UI			UI	

High Speed Mode - Rising and Falling Timings

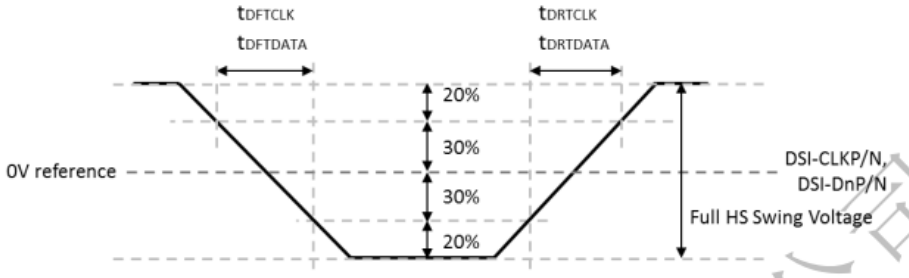


Figure 4-7 Rsing and Falling Timings

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150pS		0.3*UI		2,3
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N	150pS		0.3*UI		1,2,3
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150pS		0.3*UI		2,3
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N	150pS		0.3*UI		1,2,3

***Note* 1:** DnP/N, n =0,1,2 and 3.
***Note* 2:** The display module has to meet timing requriements,which are defined for the transmitter (MCU) on MIPI D-PHY standard.
***Note* 3:** DSI-CLK+ = CLKP, DSI-CLK- =CLKN, DSI-D0+ =D0P, DSI-D0- =D0N.

Low Speed Mode - Bus Turn Around

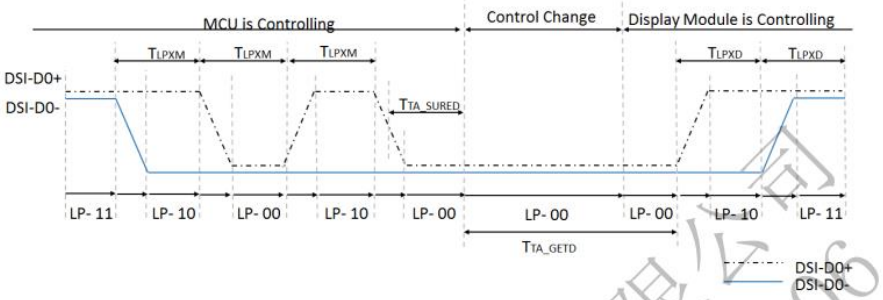


Figure 4-8 Bus Turnaround (BTA) from MCU to display module Timing

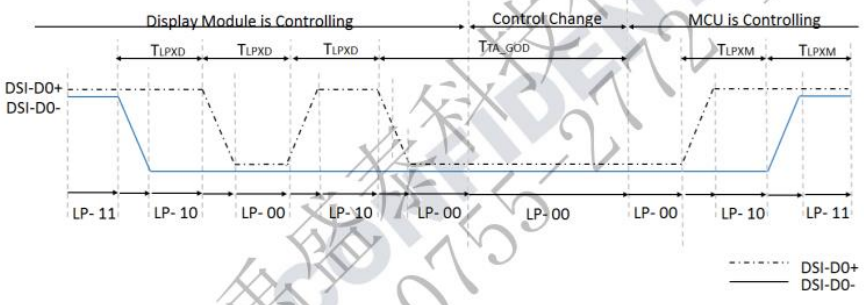


Figure 4-9 Bus Turnaround (BTA) from Display module to MCU Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
D0P/N	T_{LPXM}	Length of LP-00,LP-01,LP-10 or LP11 periods MCU to Display Module	50		75	nS	1
D0P/N	T_{LPXD}	Length of LP-00,LP-01,LP-10 or LP11 periods Display Module to MCU	50		75	nS	1
D0P/N	T_{TA_SURED}	Time-out before the Display Module starts driving	T_{LPXD}		2* T_{LPXD}	nS	1
D0P/N	T_{TA_GETD}	Time to drive LP-00 by Display Module	5* T_{LPXD}			nS	1
D0P/N	T_{TA_GOD}	Time to drive LP-00 after turnaround request -MCU	4 * T_{LPXD}			nS	1

Note 1: D0P = DSI-D0+, D0N = DSI-D0-.

Data Lanes from Low Power Mode to High Speed Mode

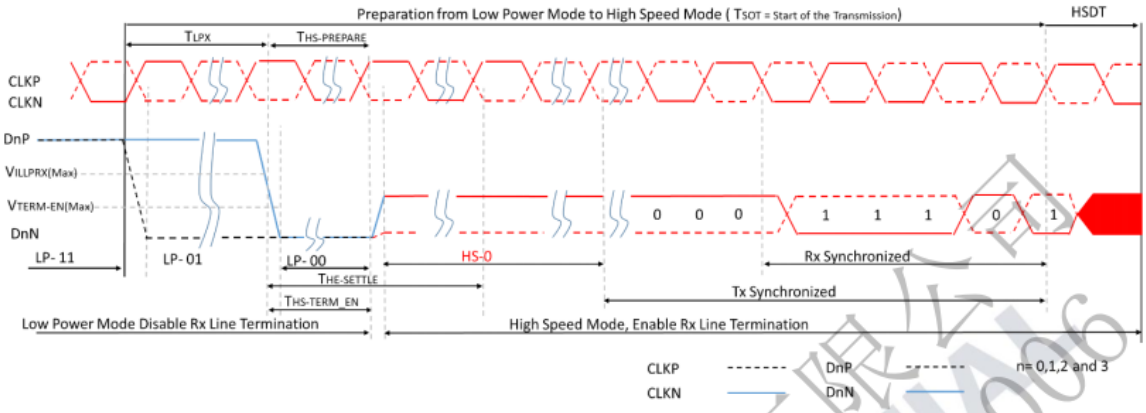
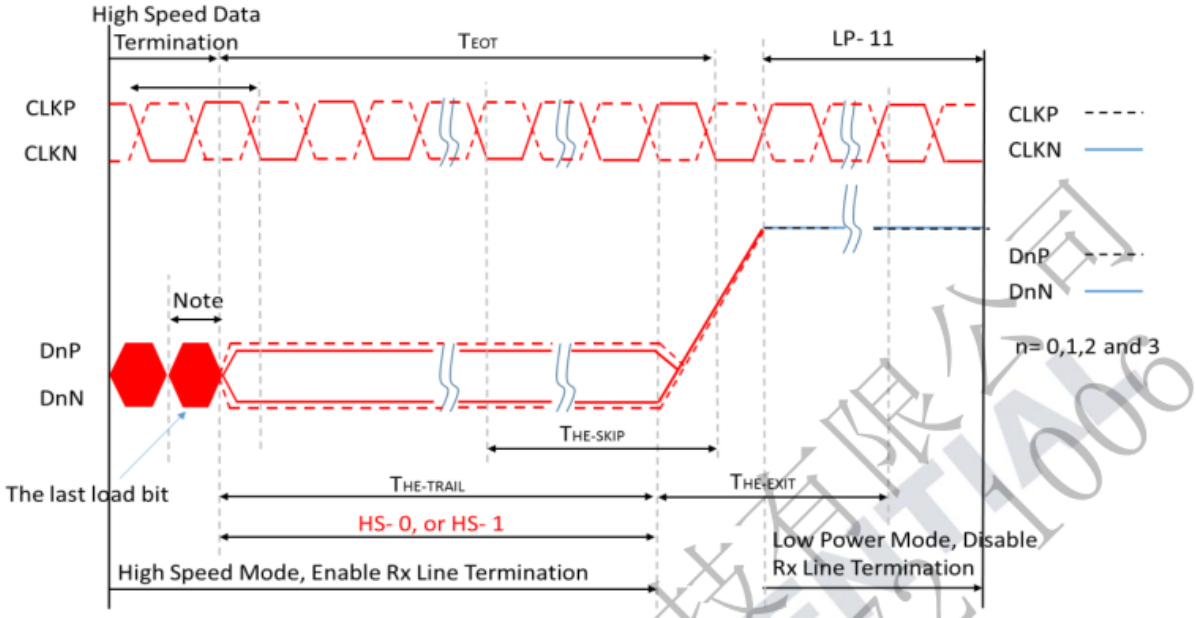


Figure 4-10 Data Lanes from Low Power Mode to High Speed Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
DnP/N	TLPX	Length of any Low Power State Period	50			nS	1
DnP/N	THS-PREPARE	Time to drive LP-00 to prepare for HS Transmission	40+4*UI		85+6*UI	nS	1
DnP/N	THS-TREM-EN	Time to enable Data lane Receiver line termination measured from when Dn crosses VILMAX			35+4*UI	nS	1

Note 1: DnP/N, n=*0,1,2 and 3.*

Data Lanes from High Speed Mode to Low Power Mode



Note:
If the last load bit is HS- 0, the transmitter changes from HS- 0 to HS- 1.
If the last load bit is HS- 1, the transmitter changes from HS- 1 to HS- 0

Figure 4-11 Data Lanes from High Speed Mode to Low Power Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
DnP/N	THS-SKIP	Time-Out at Display Module to ignore transition period of EoT	40		55+4*UI	nS	1
DnP/N	THS-EXIT	Time to drive LP-11 after HS burst	100			nS	1

Note 1: DnP/N, n=*0,1,2 and 3.*

DSI Clock Burst – High speed mode to /from Low Power Mode

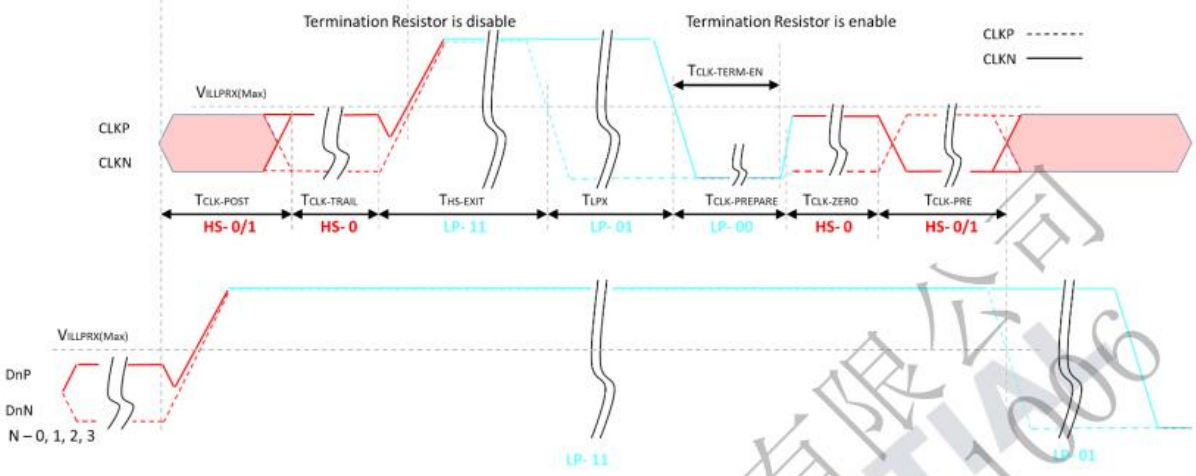


Figure 4-12 Clock Lane –High speed mode to / from Low Power Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
CKP/N	$T_{CK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52*UI			nS	
CKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60			nS	
CKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100			nS	
CKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38		95	nS	
CKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination			38	nS	
CKP/N	$T_{CLK-PREPARE}$+ $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300			nS	
CKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8*UI			nS	

Reset Timing:

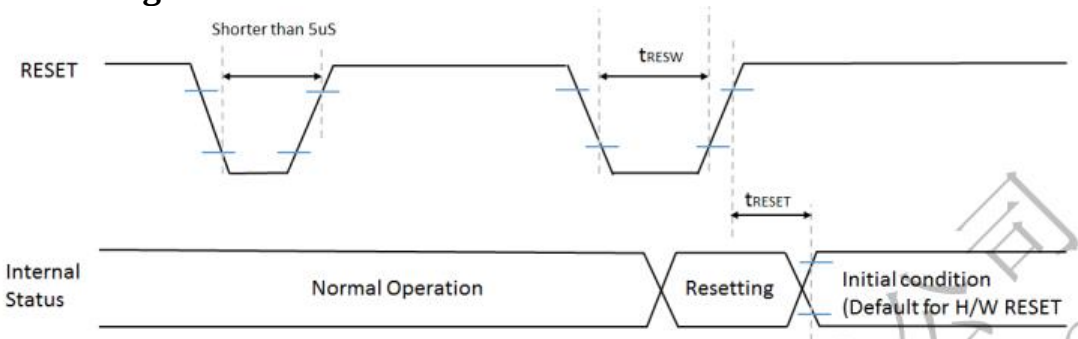


Figure 4-13 Reset Input Timing

Table 4-2 Reset Input Timing

Signal	Symbol	Parameter	Description	Specification			Unit	Notes
				MIN	TYP	MAX		
RESET	tRESW	Reset "L" pulse width		10			uS	1
	tRESET	Reset complete time	When reset applied during Sleep in mode			5	mS	2
			When reset applied during Sleep Out mode			120	mS	5

***Note* 1:** Condition : Ta =25℃.

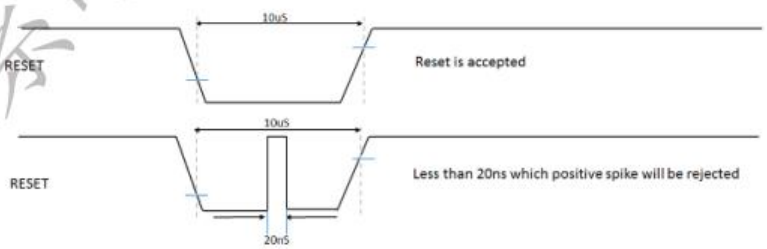
***Note* 2:** Spike due to an electrostatic discharge on RESET line does not cause irregular system reset according to the table below.

RESET Pulse	Action
Less than 5us	Reset Rejected
More than 10uS	Reset
Between 5us and 10uS	Reset Start

***Note* 2:** During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in sleep out mode. The display remains the blank state in sleep in mode) and then return to Default condition for H/W RESET.

Note3: During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W RESET complete time (tRESET) within 5ms after a rising edge of RESET.

***Note 4*:** Spike Rejection also applies during a valid reset pulse as shown below:



***Note 5*:** It is necessary to wait 5ms after releasing RESET when sending commands, and Sleep Out command can not be sent within 120ms.

Power ON Sequence

Hardware Reset would be applied when power on. The RESX is held at "H" by the host after both VCI and IOVCC have been applied. Otherwise, correct functionality will not be guaranteed. If RESX is held to "L" by the host during Power On, it must keep "L" at least 10μsec after both VCI and IOVCC applied. The power on sequence for different power input modes are shown below.

Table 7-1 Power ON Sequence Timing

Symbol	Description	Value			Unit	Remark
		Min.	Typ.	Max.		
Ton1	Delay time of IOVCC to VCI	0			ms	
Ton2	Delay time of IOVCC to VSP	0			ms	
T1	IOVCC rising time	-		2	ms	
T2	Delay time of IOVCC to valid RESX to "H"	10			ms	
T3	Delay time of RESX "H" to initial code ready	20			ms	
T4	Delay time of IOVCC (HS_VCC) to MIPI bus ready	0		T2	ms	
T5	RESX "L" period	10			us	
T6	Delay time of initial code reloaded to video packet transmit	120			ms	

Power on sequence: PCCS [1:0]=[1,0]

Applied Power: IOVCC, VCI

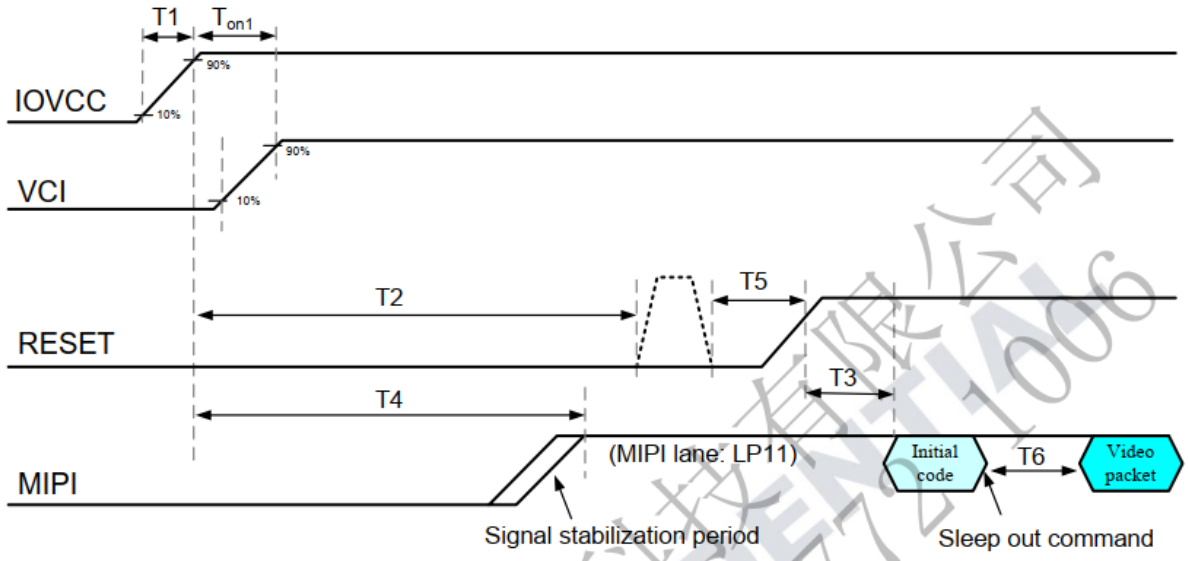


Figure 7-1 Power on sequence at PCCS[1:0]=[1,0] mode

Note1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Power on sequence: PCCS [1:0]=[1,1]

Applied Power: IOVCC, VSP, VSN

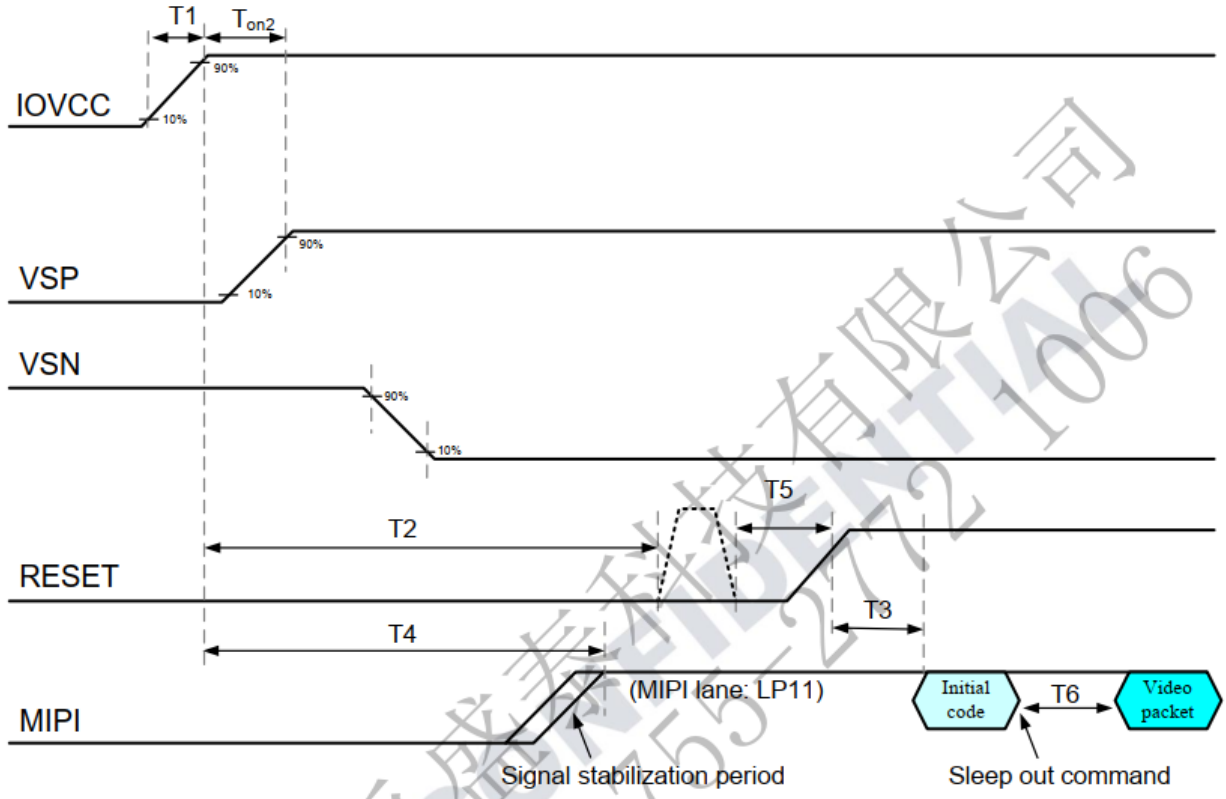


Figure 7-2 Power on sequence at PCCS[1:0]=[1,1] mode

Note1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Power OFF Sequence

Power off sequence for different PCCS-mode applications are shown below:

Table 7-2 Power OFF Sequence Timing

Symbol	Description	Value			Unit	Remark
		Min.	Typ.	Max.		
Toff1	Delay time of VCI to IOVCC	0	-	-	ms	
Toff2	Delay time of VSP to IOVCC	0	-	-	ms	
Toff3	Delay time of VSN to VSP	0	-	-	ms	
T7	IOVCC falling time	-	-	-	ms	
T8	Delay time of RESX "L" to VCI	0	-	-	us	
T9	Delay time of MIPI LP-00 to valid RESX "L"	0	-	-	us	
T10	Delay time of Sleep-in received to valid RESX "L"	100	-	-	ms	
T11	Delay time of RESX "L" to VSN	0	-	-	ms	

Power off sequence: PCCS[1:0] = [1,0]

Application Power: IOVCC, VCI,

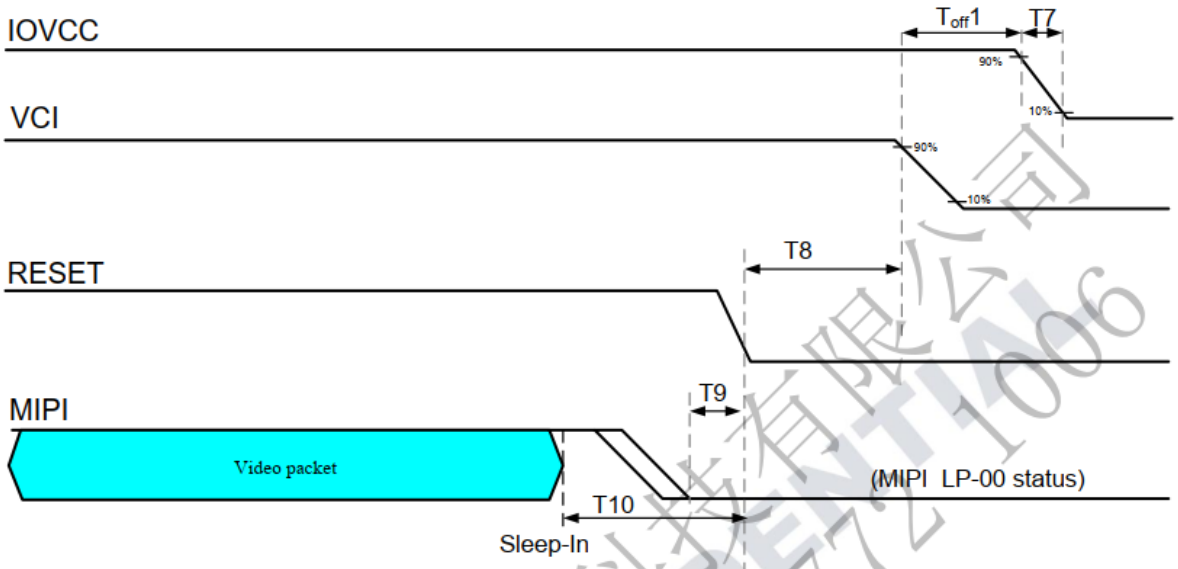


Figure 7-3 Power off sequence at PCCS[1:0]=[1,0] mode

Note1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Power off sequence: PCCS[1:0] = [1,1]

Application Power: IOVCC, VSP, VSN

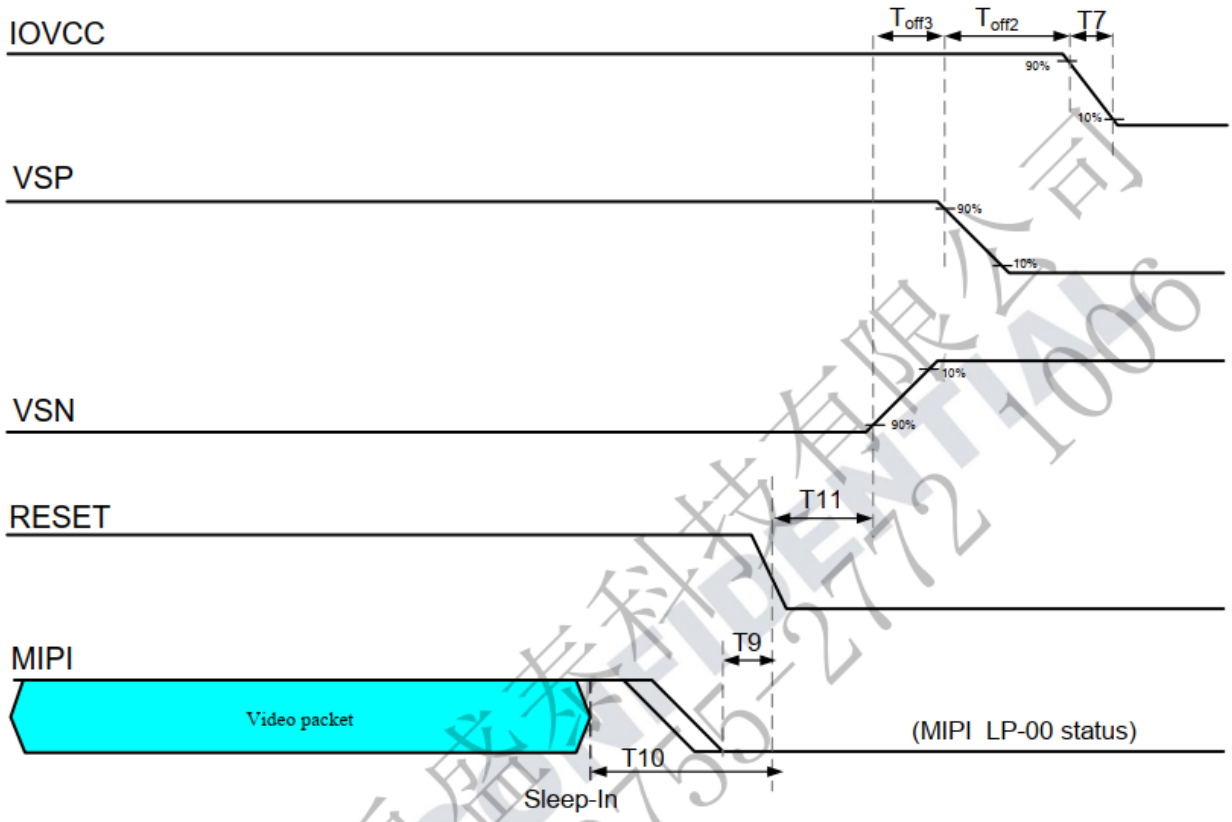


Figure 7-4 Power off sequence at PCCS[1:0]=[1,1] mode

Note1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

7. Optical Characteristics:

Item		Symbol	Conditions	Specifications			Unit	Note
				Min	Typ	Max		
Transmittance (with polarizer)		T(%)	-	4.55	4.5.35	-	-	-
NTSC		%	θ=0	55	60	-	-	-
Contrast Ratio		CR	θ=0 Normal Viewing angle	1000	1200	-	-	(1) (2)
Response time		TR+TF	-	-	30	35	ms	(1) (3)
Viewing angle	Hor.	Θx+	CR≧10	80	85	-	deg.	-
		Θx-		80	85	-		
	Ver.	Θy+		80	85	-		
		Θy-		80	85	-		

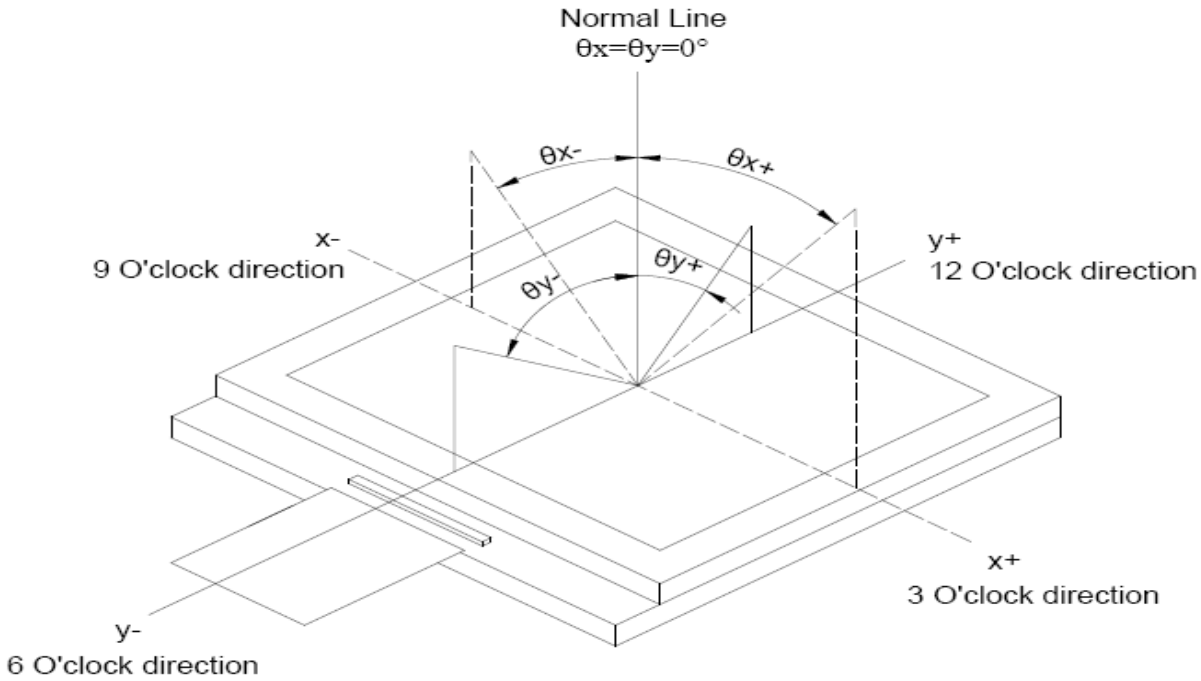
Measuring Condition

1. Measuring surrounding: dark room
2. Ambient temperature: 25±2℃
3. 30 min. Warm-up time.

Color of CIE Coordinate:

Item		Symbol	Condition	Min.	Typ.	Max.
Chromaticity Coordinates (Transmissive)	Red	x	θ = φ = 0 ° LED Backlight Color Degree	TBD	0.650	TBD
		y		TBD	0.322	TBD
	Green	x		TBD	0.280	TBD
		y		TBD	0.563	TBD
	Blue	x		TBD	0.135	TBD
		y		TBD	0.141	TBD
	White	x		TBD	0.292	TBD
		y		TBD	0.337	TBD

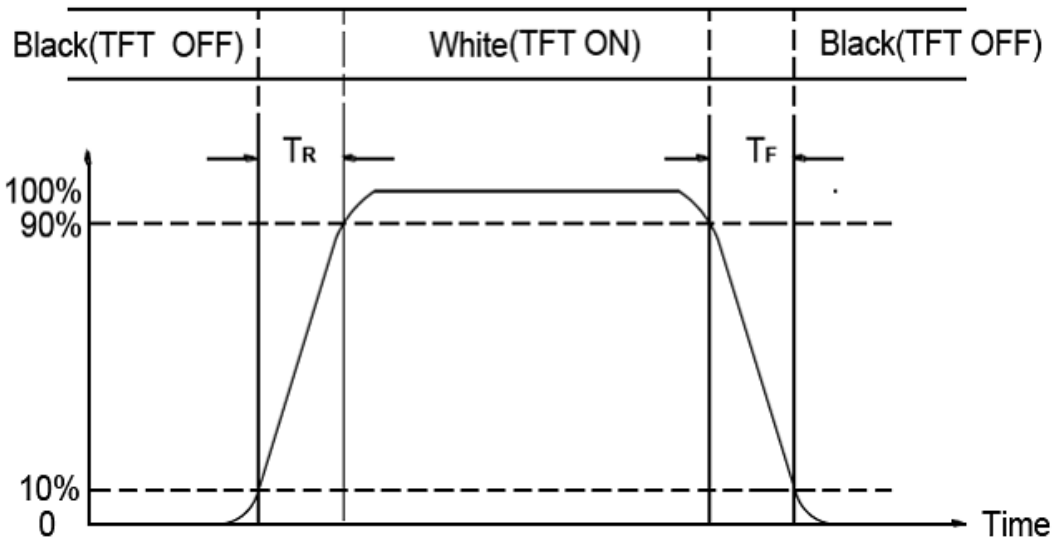
Note (1) Definition of Viewing Angle :



Note (2) Definition of Contrast Ratio(CR) :
measured at the center point of panel

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black}}$$

Note (3) Definition of Response Time : Sum of TR and TF

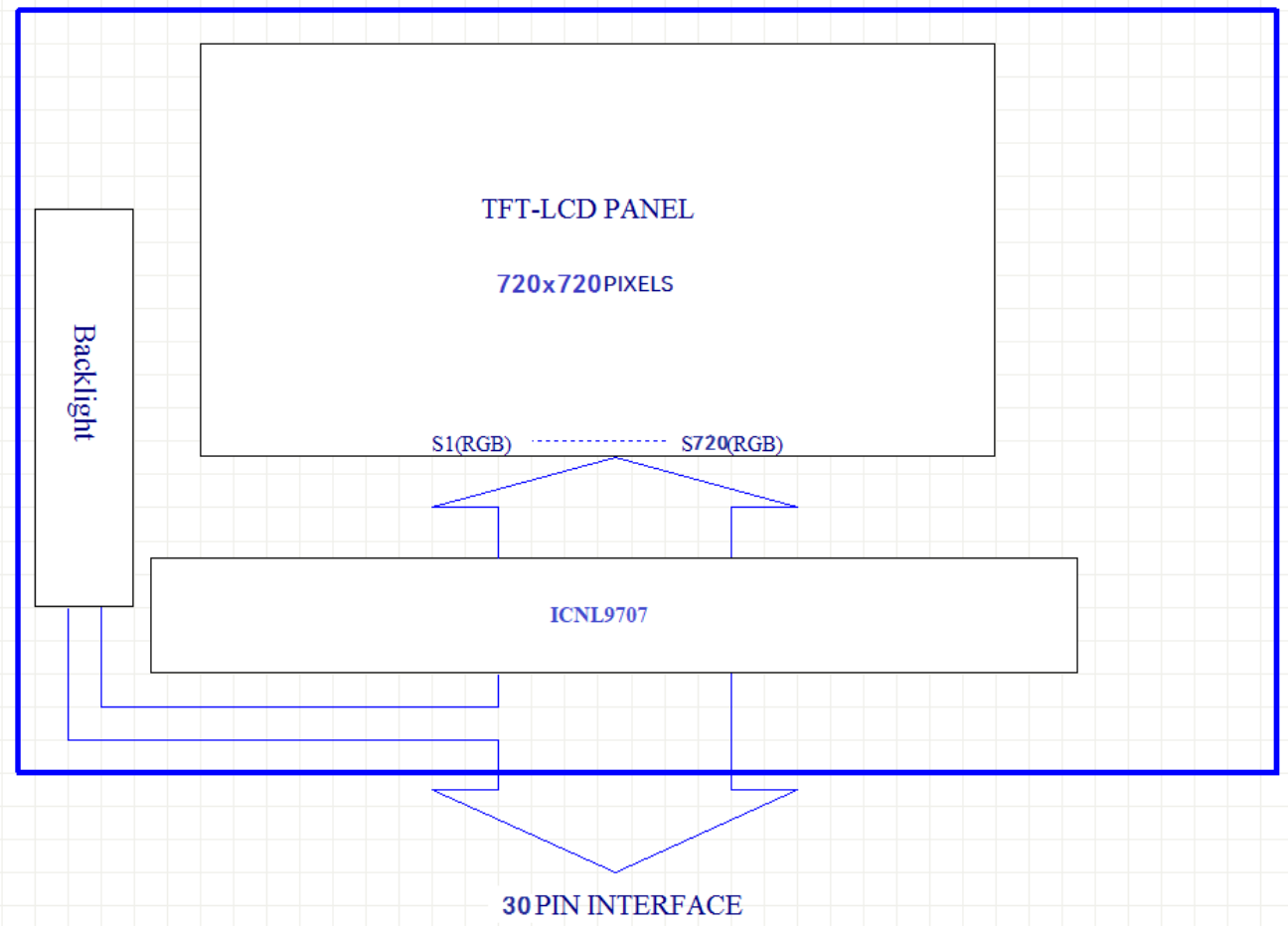


8. Interface Pin Assignment:

8-1 LCM FPC Interface

No.	Symbol	Function
1	GND	Ground
2	VCI	Power Supply
3	VCI	Power Supply
4	GND	Ground
5	GND	Ground
6	VDDI	Power Supply
7	VDDI	Power Supply
8	GND	Ground
9	RESET	Reset signal input terminal .
10	GND	Ground
11	D3P	High speed interface data differential signal input/output pins
12	D3N	High speed interface data differential signal input/output pins
13	GND	Ground
14	D2P	High speed interface data differential signal input/output pins
15	D2N	High speed interface data differential signal input/output pins
16	GND	Ground
17	CLKP	High speed interface clock differential signal input pins
18	CLKN	High speed interface clock differential signal input pins
19	GND	Ground
20	D1P	High speed interface data differential signal input/output pins
21	D1N	High speed interface data differential signal input/output pins
22	GND	Ground
23	D0P	High speed interface data differential signal input/output pins
24	D0N	High speed interface data differential signal input/output pins
25	GND	Ground
26	LEDA	LED anode
27	LEDA	LED anode
28	LEDK	LED cathode
29	LEDK	LED cathode
30	GND	Ground

9. Block Diagram:



10. Backlight:

1. Standard Lamp Styles (Edge Lighting Type):
The LED chips are distributed over the edge light area of the illumination unit, which gives the less power consumption:

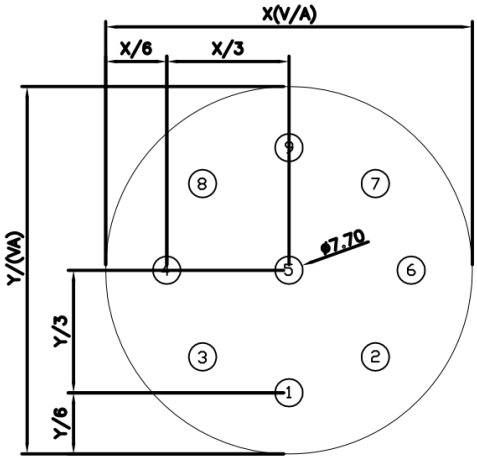
2. The Main Advantages of the LED Backlight are as following:
2.1 The brightness of the backlight can simply be adjusted.
By a resistor or a potentiometer.

3. Data About LED Backlight: (Ta=25°)

PARAMETER	Sym.	Min.	Typ.	Max.	Unit	Test Condition	Note
Supply Current	I		20		mA		
Supply Voltage	V	18.9	21.7	23.8	V	If=20mA	
Luminous Intensity for LCM	IV	350	400	-	cd/m2		2
Uniformity for LCM	-	70	-	-	%		3
Life Time	-	50000	-	-	Hr.		4
Color	White						

NOTE:
1. Backlight Only
2. Average Luminous Intensity of P1-P5
3. Uniformity = Min/Max * 100%
4. LED life time defined as follow: the final brightness is at 50% of original brightness

Measured Method: (X*Y: Light Area)



Internal Circuit Diagram

(Effective spatial Distribution)
Using aperture of 1 °,distance 50cm

11. Standard Specification for Reliability .:

11–1. Standard Specifications for Reliability of LCD Module

No	Item	Description
01	High temperature operation	The sample should be allowed to stand at 85℃ for 120 hours under driving condition and then returning it to normal temperature condition, and allowing it stand for 2 hours.
02	Low temperature operation	The sample should be allowed to stand at -30℃ for 120 hours under driving condition and then returning it to normal temperature condition, and allowing it stand for 2 hours.
03	High temperature storage	The sample should be allowed to stand at 85℃ for 240 hours under no-load condition, and then returning it to normal temperature condition, and allowing it stand for 2 hours.
04	Low temperature storage	The sample should be allowed to stand at -30℃ for 240 hours under no-load condition, then returning it to normal temperature condition, and allowing it stand for 2 hours.
05	Moisture storage	The sample should be allowed to stand at 60℃,90%RH MAX for 240 hours under no-load condition, then taking it out and drying it at normal temperature for 2 hours.
06	Thermal shock storage	The sample should be allowed to stand the following 10 cycles : -30℃ for 30 minutes → normal temperature for 5 minutes → +85℃ for 30 minutes → normal temperature for 5 minutes, as one cycle.
07	Packing vibration	Frequency range : 10Hz ~ 55Hz Amplitude of vibration : 1.5mm Sweep time: 12 min X,Y,Z 2 hours for each direction.
08	Packing drop test	According to ISTA 1A 2001.
09	Electrical Static Discharge	Air: ±6KV 150pF/330Ω 5 times
		Contact: ±4KV 150pF/330Ω 5 time

*Sample size for each test item is 3~5pcs

11 - 2. Testing Conditions and Inspection Criteria

For the final test the testing sample must be stored at room temperature for 24 hours, after the tests listed in Table 12.2, Standard specifications for Reliability have been executed in order to ensure stability.

No	Item	Test Model	In section Criteria
01	Current Consumption	Refer To Specification	The current consumption should conform to the product specification.
02	Contrast	Refer To Specification	After the tests have been executed, the contrast must be larger than half of its initial value prior to the tests.
03	Appearance	Visual inspection	Defect free.

11- 3. MTBF

MTBF	Functions, performance, appearance, etc. shall be free from remarkable deterioration within 50,000 hours under ordinary operating and storage conditions room temperature (25±5℃), normal humidity (50±10% RH), and in area not exposed to direct sun light.

12. Specification of Quality Assurance:

12-1. Purpose

This standard for Quality Assurance should affirm the quality of LCD module products to supply to purchaser by YEEBO CORPORATION (Supplier).

12-2. Standard for Quality Test

a. Inspection:

Before delivering, the supplier should take the following tests, and affirm the quality of product.

b. Electro-Optical Characteristics:

According to the individual specification to test the product.

c. Test of Appearance Characteristics:

According to the individual specification to test the product.

d. Test of Reliability Characteristics:

According to the definition of reliability on the specification for testing products.

e. Delivery Test:

Before delivering, the supplier should take the delivery test.

(i) Test method: According to **ISO2859-1.**General Inspection Level Ⅱ take a single time.

(ii) The defects classify of AQL as following:

Major defect: AQL = 0.65

Minor defect: AQL = 2.5

Total defects: AQL = 2.5

12-3. Non- conforming Analysis & Deal With Manners

a. Non- conforming Analysis:

(i) Purchaser should supply the detail data of non- conforming sample and the non-conforming.

(ii) After accepting the detail data from purchaser, the analysis of non- conforming should be finished in two weeks.

(iii) If supplier can not finish analysis on time, must announce purchaser before 3 days.

b. Disposition of non- conforming:

(i) If find any product defect of supplier during assembly time, supplier must change the good product for every defect after recognition.

(ii) Both supplier and customer should analyze the reason and discuss the disposition of non- conforming when the reason of nonconforming is not sure.

12-4. Agreement items

Both sides should discuss together when the following problems happen.

a. There is any problem of standard of quality assurance, and both sides should think that must be modified.
b. There is any argument item which does not record in the standard of quality assurance.
c. Any other special problem.

12-5. Standard of The Product Appearance Test

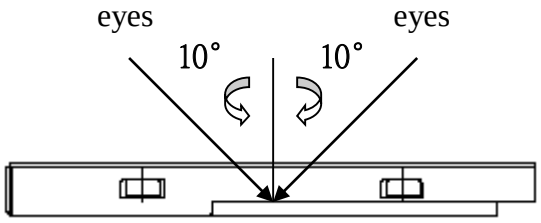
a. Manner of appearance test:

(i) The test must be under 20W ×2 or 40W fluorescent light, and the distance of view must be at 30±5cm.

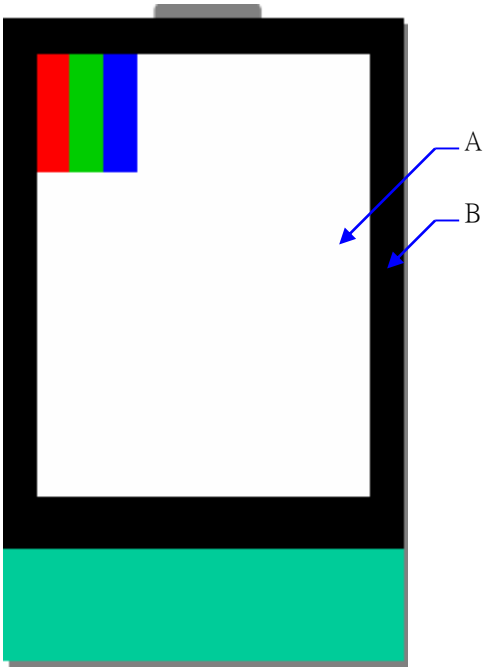
(ii) When test the model of transmissive product must add the reflective plate.

(iii)The test direction is base on around 10 °of vertical line.

(iiii)Temperature: 25±5℃ Humidity: 60±10%RH



(iv) Definition of area:



A. Area: Viewing area.

B. Area: Out of viewing area.
(Outside viewing area)

b. Basic principle:

(i) It will accord to the AQL when the standard can not be described.

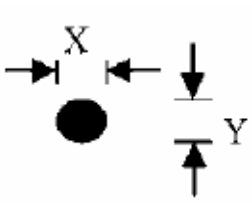
(ii) The sample of the lowest acceptable quality level must be discussed by both supplier and customer when any dispute happened.

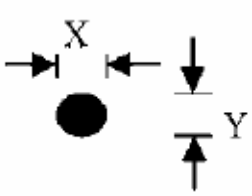
(iii) Must add new item on time when it is necessary.

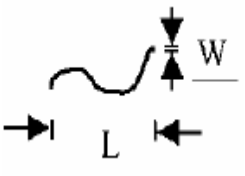
c. Standard of inspection: (Unit: mm)

12-6. Inspection specification

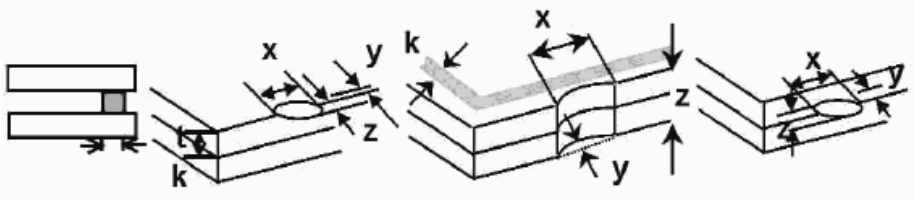
Defect out of viewing area can be neglected.

<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>01</td><td>Electrical Testing</td><td>1.1 Missing vertical, horizontal segment, segment contrast defect.
1.2 Missing character, dot or icon.
1.3 Display malfunction.
1.4 No function or no display.
1.5 Current consumption exceeds product specifications.
1.6 LCD viewing angle defect.
1.7 Mixed product types.
1.8 Flicker</td><td>0.65</td></tr>
<tr><td>02</td><td>Black or White spots or Bright spots or Color spots on LCD (Display only)</td><td>2.1 Dot dimension as below drawing:
Φ = (X+Y) / 2
 

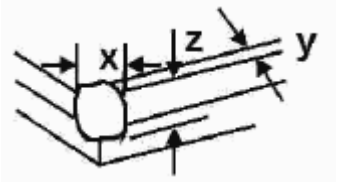
<table><tr><th>Size(mm)</th><th>Acceptable Q'ty</th></tr><tr><td>Φ≦0.20</td><td>Accept no dense</td></tr><tr><td>0.20< Φ≦0.40</td><td>5</td></tr><tr><td>0.40< Φ</td><td>0</td></tr></table>
2.2 Not visible through 5% ND filter
* Densely spaced: No more than two spots within 3mm.</td><td>2.5</td></tr>
<tr><td rowspan="2">03</td><td rowspan="2">LCD and Touch Panel black spots, white spots, contamination (non – display)</td><td>3.1 Round type: As following drawing
Φ = (X+Y) / 2
 

<table><tr><th>Size(mm)</th><th>Acceptable Q'ty</th></tr><tr><td>Φ≦0.20</td><td>Accept no dense</td></tr><tr><td>0.20< Φ≦0.40</td><td>5</td></tr><tr><td>0.40< Φ</td><td>0</td></tr></table>
* Densely spaced: No more than two spots within 3mm.</td><td>2.5</td></tr>
<tr><td>3.2 Line type: (As following drawing)
 

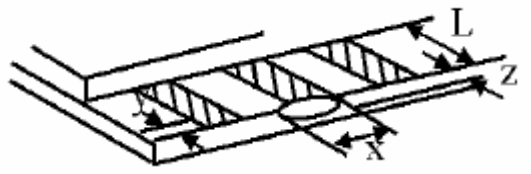
<table><tr><th>Length(mm)</th><th>Width(mm)</th><th>Acceptable Q'ty</th></tr><tr><td>L≦10</td><td>W≦0.1</td><td>Accept no dense</td></tr><tr><td>L≦10.0</td><td>0.1<W≦0.25</td><td>4</td></tr><tr><td>L>10</td><td>----</td><td>Rejection</td></tr><tr><td>----</td><td>0.25<W</td><td>Rejection</td></tr></table>
* Densely spaced: No more than two lines within 3mm.</td><td>2.5</td></tr>
</table>

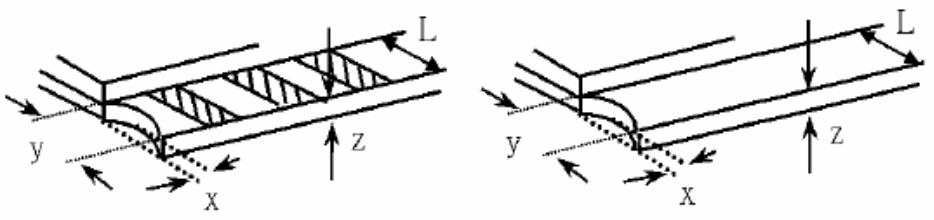
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>04</td><td>Polarizer bubbles</td><td>If bubbles are visible, judge using black spot specifications, not easy to find, must check in specify direction
<table>
<tr><td>Size Φ(mm)</td><td>Acceptable Q'ty</td></tr>
<tr><td>Φ≦0.20</td><td>Accept no dense</td></tr>
<tr><td>0.20< Φ≦0.50</td><td>4</td></tr>
<tr><td>0.50< Φ≦1.00</td><td>3</td></tr>
<tr><td>1.00< Φ</td><td>0</td></tr>
<tr><td>Total Q’ty</td><td>4</td></tr>
</table></td><td>2.5</td></tr>
<tr><td>05</td><td>Scratches</td><td>Follow NO.3 -2 Line Type.</td><td></td></tr>
<tr><td>06</td><td>Mura</td><td>Not visible through 5% ND filter in 50% gray.</td><td>2.5</td></tr>
<tr><td>07</td><td>Chipped glass</td><td>Symbols:
x: Chip length y: Chip width z: Chip thickness
k: Seal width t: Glass thickness a: LCD side length
L: Electrode pad length
7.1 General glass chip:
7.1.1 Chip on panel surface and crack between panels:
 

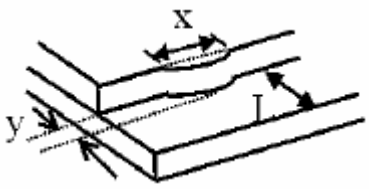
<table>
<tr><td>z: Chip thickness</td><td>y: Chip width</td><td>x: Chip length</td></tr>
<tr><td>Z≦1/2t</td><td>Not over viewing area</td><td>x≦1/8a</td></tr>
<tr><td>1/2t< z≦2t</td><td>Not exceed 1/3k</td><td>x≦1/8a</td></tr>
</table>
⊙ Unit: mm
⊙ If there are 2 or more chips, x is the total length of each chip

7.1.2 Corner crack:
 

<table>
<tr><td>z: Chip thickness</td><td>y: Chip width</td><td>x: Chip length</td></tr>
<tr><td>Z≦1/2t</td><td>Not over viewing area</td><td>x≦1/8a</td></tr>
<tr><td>1/2t< z≦2t</td><td>Not exceed 1/3k</td><td>x≦1/8a</td></tr>
</table>
⊙ Unit: mm
⊙ If there are 2 or more chips, x is the total length of each chip</td><td>2.5</td></tr>
</table>

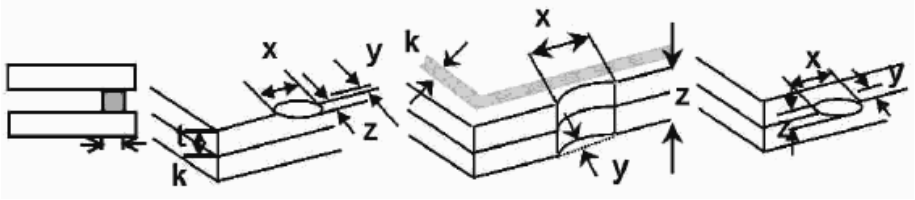
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>08</td><td>Glass crack</td><td>
Symbols:
x: Chip length y: Chip width z: Chip thickness
k: Seal width t: Glass thickness a: LCD side length
L: Electrode pad length
8.1 Protrusion over terminal:
8.1.1 Chip on electrode pad:


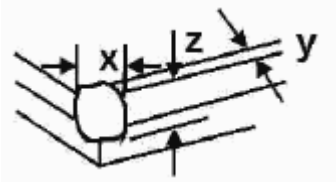
<table>
<tr><th>y: Chip width</th><th>x: Chip length</th><th>z: Chip thickness</th></tr>
<tr><td>y≦0.5mm</td><td>x≦1/8a</td><td>0< z≦t</td></tr>
</table>
8.1.2 Non-conductive portion:


<table>
<tr><th>y: Chip width</th><th>x: Chip length</th><th>z: Chip thickness</th></tr>
<tr><td>y≦L</td><td>x≦1/8a</td><td>0< z≦t</td></tr>
</table>
⊙ If there chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications.
⊙ If the product will be heat sealed by the customer, the alignment mark must mot be damaged.
8.1.3 Substrate protuberance and internal crack


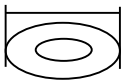
<table>
<tr><th>y: width</th><th>x: length</th></tr>
<tr><td>y≦1/3L</td><td>X≦a</td></tr>
</table>
</td><td>2.5</td></tr>
</table>

NO	Item	Criterion	AQL
09	Cracked glass	The LCD with extensive crack is not acceptable.	2.5
10	Backlight elements	10.1 Illumination source flickers when lit. 10.2 Spots or scratches that appear when lit must be judged. Using LCD spot, lines and contamination standards. 10.3 Backlight doesn't light or color is wrong.	2.5 2.5 0.65
11	Bezel	Bezel must comply with product specifications.	2.5
12	PCB、COB	12.1 COB seal may not have pinholes larger than 0.2mm or contamination. 12.2 COB seal surface may not have pinholes through to the IC. 12.3 The height of the COB should not exceed the height indicated in the assembly diagram. 12.4 There may not be more than 2mm of sealant outside the seal area on PCB. And there should be no more than three places. 12.5 Parts on PCB must be the same as on the production characteristic chart, There should be no wrong parts, missing parts or excess parts. 12.6 The jumper on the PCB should conform to the product characteristic chart. 12.7 PCBA cosmetic control base on latest IPC standard,IPC-A-610,acceptalbe limit of grade 2.	2.5 2.5 2.5 2.5 0.65 0.65 2.5
13	FPC	13.1 FPC terminal damage ≦ 1/2 FPC terminal width and can not affect the function , we judge accept. 13.2 FPC alignment hole damage ≦ 1/2 alignment area and can not affect the function , we judge accept.	2.5 2.5
14	Soldering	14.1 No cold solder joints, missing solder connections, oxidation or icicle. 14.2 No short circuits in components on PCB or FPC.	2.5 0.65

<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>15</td><td>Touch Panel Chipped glass</td><td>
Symbols:
x: Chip length y: Chip width z: Chip thickness
k: Seal width t: Touch Panel Total thickness a: LCD side length
L: Electrode pad length
15.1 General glass chip:
15.1.1 Chip on panel surface and crack between panels:


<table>
<tr><th>z: Chip thickness</th><th>y: Chip width</th><th>x: Chip length</th></tr>
<tr><td>Z≦t</td><td>≦1/2 k and not over viewing area</td><td>x≦1/8a</td></tr>
</table>
⊙ Unit: mm
⊙ If there are 2 or more chips, x is the total length of each chip
15.1.2 Corner crack:


<table>
<tr><th>z: Chip thickness</th><th>y: Chip width</th><th>x: Chip length</th></tr>
<tr><td>z≦t</td><td>≦1/2 k and not over viewing area</td><td>x≦1/8a</td></tr>
</table>
⊙ Unit: mm
⊙ If there are 2 or more chips, x is the total length of each chip
</td><td>2.5</td></tr>
</table>

<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>16</td><td>Touch Panel(Fish eye)</td><td>
<table>
<tr><th>SIZE(mm)</th><th>Acceptable Q’ty</th></tr>
<tr><td>L≦0.7</td><td>Accept no dense</td></tr>
<tr><td>L>0.7mm</td><td>0</td></tr>
</table>
L

</td><td>2.5</td></tr>
<tr><td>17</td><td>Touch Panel Newton ring</td><td>Newton ring dimension ≦ 1/2 touch panel area and not affect font and line distortion(≦2.5%) , it is acceptable.</td><td>2.5</td></tr>
<tr><td>18</td><td>Touch Panel Linearity</td><td>Less than 2.5% is acceptable.</td><td>2.5</td></tr>
<tr><td>19</td><td>LCD Ripple</td><td>Touch the touch panel , can not see the LCD ripple.
Pen: R 1.0mm silicon rubber.
Operation Force: 80g</td><td>2.5</td></tr>
<tr><td>20</td><td>General appearance</td><td>20.1 Pin type must match type in specification sheet.
20.2 LCD pin loose or missing pins.
20.3 Product packaging must the same as specified on packaging specification sheet.
20.4 Product dimension and structure must conform to product specification sheet.</td><td>0.65
0.65
0.65
0.65</td></tr>
</table>

13. Handling Precaution:

13-1 Handling of LCM

- Don't give external shock.
- Don't apply excessive force on the surface.
- Liquid in LCD is hazardous substance. Must not lick and swallow. when the liquid is attach to your hand, skin, cloth etc. Wash it out thoroughly and immediately.
- Don't operate it above the absolute maximum rating.
- Don't disassemble the LCM.
- The operators should be grounded whenever he/she comes into contact with the module. Never touch any of the conductive parts such as the LSI pads,the copper leads on the PCB and the interface terminals with any parts of the human body.
- The modules should be kept in antistatic bags or other containers resistant to static for storage.
- The module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

13-2 Storage

- Store in an ambient temperature of 25±10℃, and in a relative humidity of 50±10%RH. Don't expose to sunlight or fluorescent light.
- Storage in a clean environment, free from dust, active gas, and solvent.
- Store in anti-static electricity container.
- Store without any physical load.

13-3 Soldering

- Use only soldering irons with proper grounding and no leakage.
- Iron: No higher than 310±10℃ and less than 3 sec during Hand soldering.
- Rewiring: no more than 2 times.

14. Warranty

This product has been manufactured to specifications as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we will not take responsibility if the product is used in medical devices, nuclear power control equipment, aerospace equipment, fire and security systems, or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required. If the product is to be used in any of the above applications, we will need to enter into a separate product liability agreement.

1. We cannot accept responsibility for any defect arise after additional process of the product (including disassembly and reassembly), after product delivery.
2. We cannot accept responsibility for any defect, which may arise after the application of strong external force to the product.
3. We cannot accept responsibility for any defect, which may arise due to the application of static electricity after the product has passed your company's acceptance inspection procedures.
4. We can not accept responsibility for industrial property, which may arise through the use of your product , with exception to those issues relating directly to the structure or method of manufacturing of our product within one year from YEEBO shipment.
5. For Heatseal Product which required to heatseal by customer side, parts must be used within three months after delivery from factory.
6. For TAB Product which required to solder by customer side, parts must be used within three months after delivery from factory.
7. The liability of YB is limited to repair or replacement on the terms set forth below. YB will not be responsible for any subsequent or consequential events or injury or damage to any personnel or user including third party personnel and/or user. Unless otherwise agreed in writing between YB and the customer, YB will only replace or repair any of its LCD which is found defective electrically or visually when inspected in accordance with YB GENERAL LCD INSPECTION STANDARD.

15. Guarantee:

Our products meet requirements of the environment.
YEEBO ROHS requirement is based on European Union Directive 2011/65/EU (ROHS) Requirements and Update.