SPECIFICATION
FOR
LCD MODULE

MODULE NO: YB-TG176220S12A-N-A0

Doc.Version:04

Customer Approval:

☐ Accept ☐ Reject

YEEBO	NAME	SIGNATURE	DATE
Prepare	Electronic Engineer		2015.10.20
Check	Mechanical Engineer	楊仁豪	2015.10.20
Verify			2015.10.20
Approval			2015.10.20

☐ APPROVAL FOR SPECIFICATIONS ONLY

■ APPROVAL FOR SPECIFICATIONS AND SAMPLE

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1. Revision History

Sample Version	DOC. Version	DATE	DESCRIPTION		CHANGED BY
A0	00	2013-11-22	SPEC ONLY	First issue	Wes/Calamie
A0	01	2013-12-13	SPEC ONLY	Update Dimension P5.	Wes/Calamie
A0	02	2014-02-06	FULL SPEC	First sample	Wes/Calamie
A0	03	2015-07-16	FULL SPEC	Modify Backlight (P16) 1.Ta=25℃ 2.Life Time=50000Hr. 3.NOTE 4. 50%	Shien/YANG
A0	04	2015-10-20	FULL SPEC	Modify 1. Module Numbering System(P3) 2. Module LCM drawing(P5) 3. Definition of Viewing Angle(P11) 4.Backlight (P16)	Shien/YANG

2. Table of Contents:

3. Module Numbering System:

(Example)

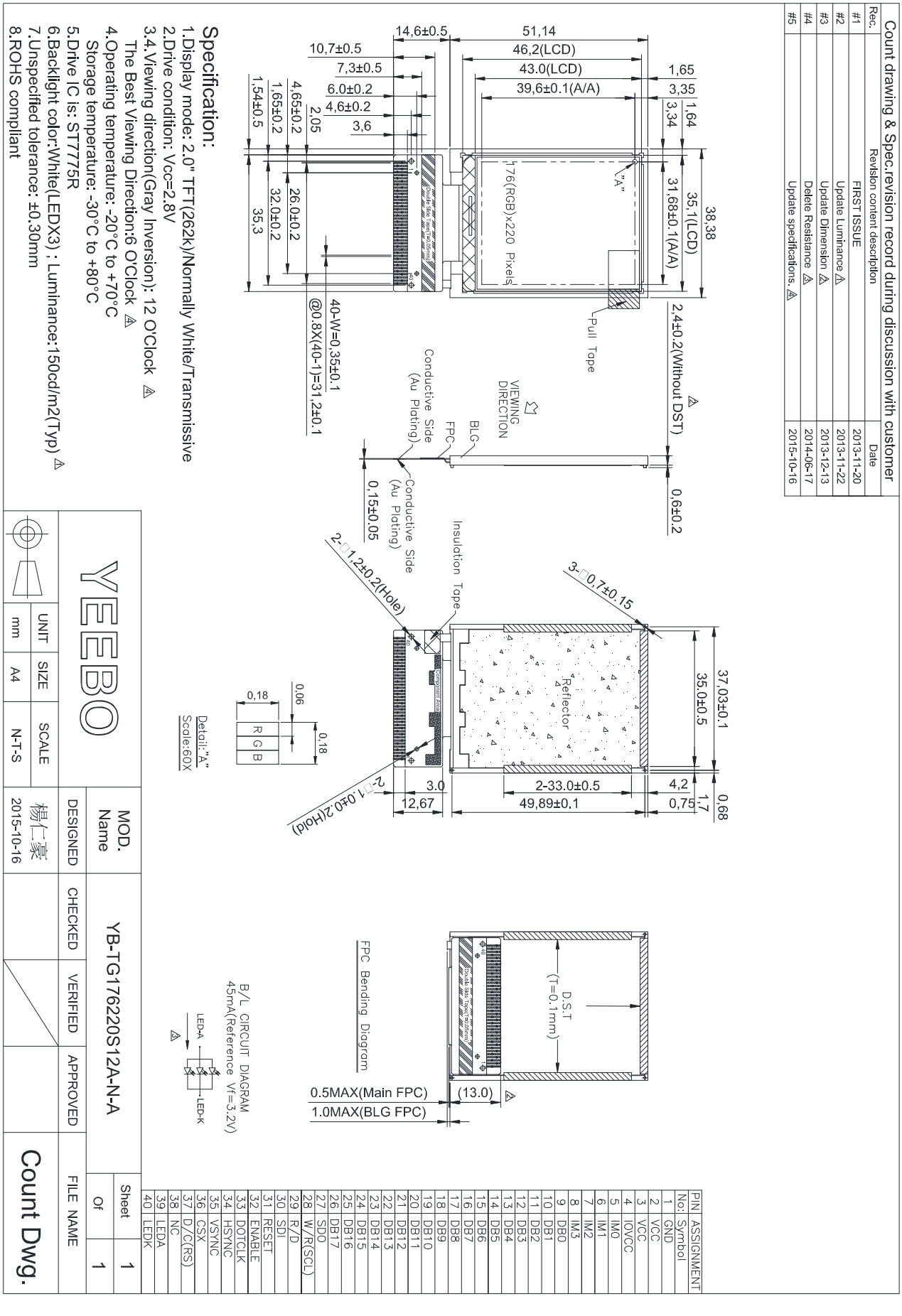
YB- T G 240320 S 01 D -T – A0

- A0: Sample Version: A0~Z0
- T: T: With Resistive Touch panel
C: With Capacitive Touch panel
N: Without Touch panel
- D: Version: A~Z
- 01: Serial No: 01~99
- S: S: STD Product
C: Customer Made
- 240320: Display Function:
Segment Number of Segment Characters Lines of Character
Column and Row of Graphic
Length * Width of Other
- G: LCM Display Type
C: Character Type；
G: Graphic Type；
GB: Graphic Black/White Type；(For E-paper)
GC: Graphic Color Type；(For E-paper)
S: Segment Type
- T: LCD Model:
C: CSTN; T: TFT; L: LTPS; O: OLED;
P: PLED; S: B/W STN; E: E-paper ;
Y: Yeetek; N: Others;
- YB: YEEBO

4. General Specification:

ITEM	CONTENTS
Module Size	38.38 (W) * 51.14 (H) * 2.4 (T) mm
Module Size(With FPC)	38.38 (W) * 65.74 (H) * 2.4 (T) mm
Display Size (Diagonal)	2.0 inch
Display Format	176(RGB)* 220 Pixels
Active Area	31.68 (W) * 39.6 (H) mm
Dots Pitch	0.18 * 0.18 mm
LCD Type	TFT (262K)/ Transmissive / Normal White
View Direction (Gray Inversion)	12 O'clock
The Best Viewing Direction	6 O'clock
Controller IC	ST7775R
Weight	6.9g

5. LCM drawing:



6. Electrical Characteristics

6-1 Absolute Maximum Ratings (Ta=25℃ VSS=0V)

Item	Symbol	Min.	Type	Max.	Unit	Remark
Power Supply voltage	VCC	-0.3		+4.6	Volt	
	IOVCC	-0.3	-	+4.6	Volt	
Operating Temperature	Topr	-20	-	+70	℃	
Storage Temperature	Tstg	-30	-	+80	℃	

Note: Absolute maximum rating is the limit value beyond which the IC maybe broken.

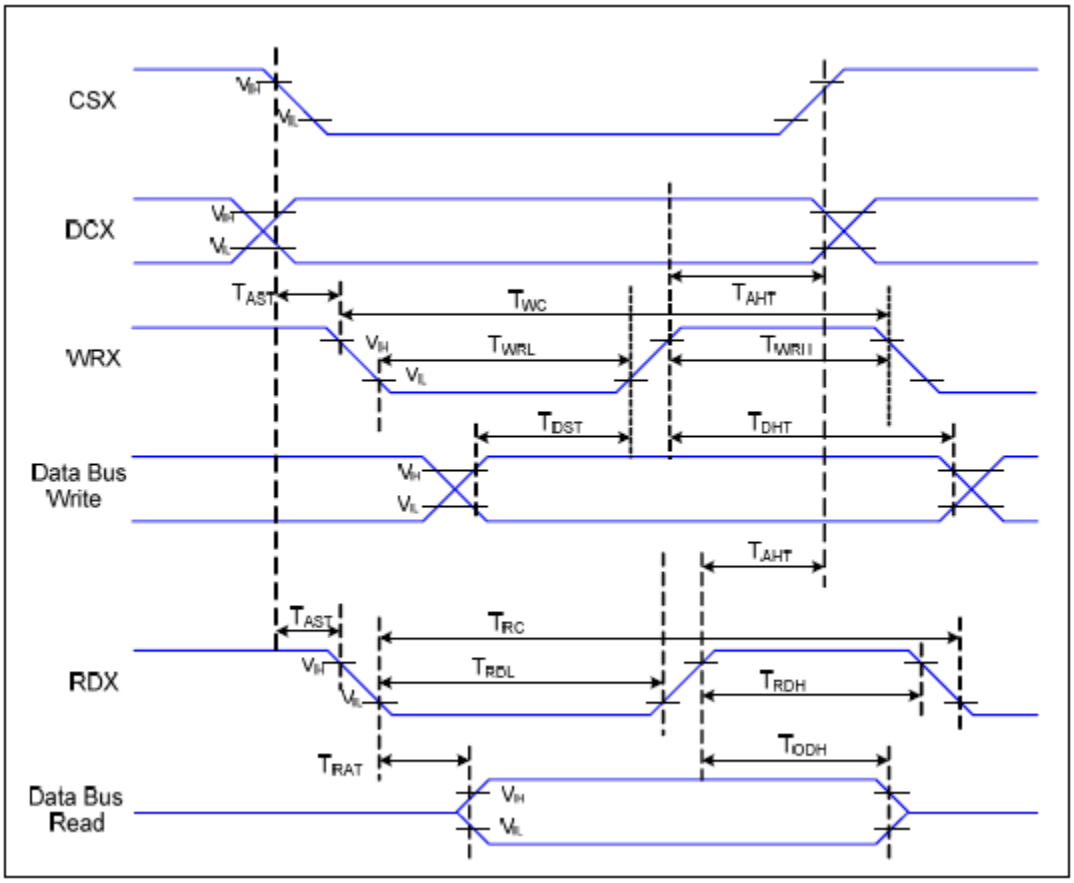
6-2 Operating Conditions (Ta=25℃)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply voltage	VCC	-	2.6	2.8	3.0	Volt
	IOVCC		2.6	2.8	3.0	Volt
Level Input Voltage	VIH	-	0.8*IOVCC	-	IOVCC	Volt
	VIL	-	GND	-	0.2*IOVCC	Volt
	VOH	-	0.8*IOVCC	-	IOVCC	Volt
	VOL	-	GND	-	0.2*IOVCC	Volt
Power Supply Current for LCM	ICC	VCC=2.8V	-	3.8	5.8	mA

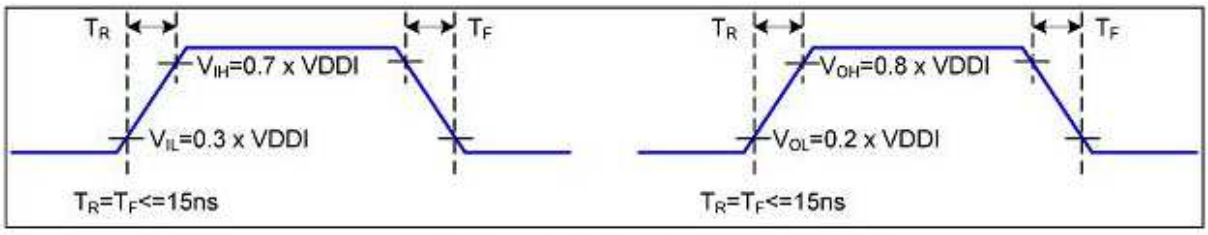
Note:GND=0V

6-3 Timing Characteristics(Reference to IC: ST7775R)

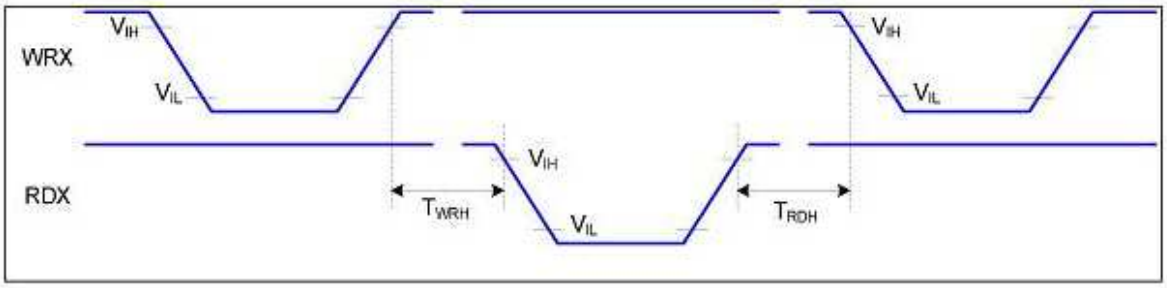
8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus



Signal	Symbol	Parameter	Min	Max	Unit	Description
DCX	TAST	Address Setup Time	10	-	ns	
	TAHT	Address Hold Time (Write/Read)	5	-	ns	
WRX	TWC	Write Cycle	70	-	ns	
	TWRH	Control Pulse "H" Duration	35	-	ns	
	TWRL	Control Pulse "L" Duration	35	-	ns	
RDX	TRC	Read Cycle (ID)	300	-	ns	When Read ID Data
	TRDH	Control Pulse "H" Duration (ID)	150	-	ns	
	TRDL	Control Pulse "L" Duration (ID)	150	-	ns	
DB[17:0]	TDST	Data Setup Time	10	-	ns	TRAT, TRATFM: 3K ohm Pull up or Down and 30pF Parallel Cap. To GND. TODH: 3K ohm Pull up or Down.
	TDHT	Data Hold Time	15	-	ns	
	TRAT	Read Access Time (ID)	-	100	ns	
	TODH	Output Disable Time	50	-	ns	



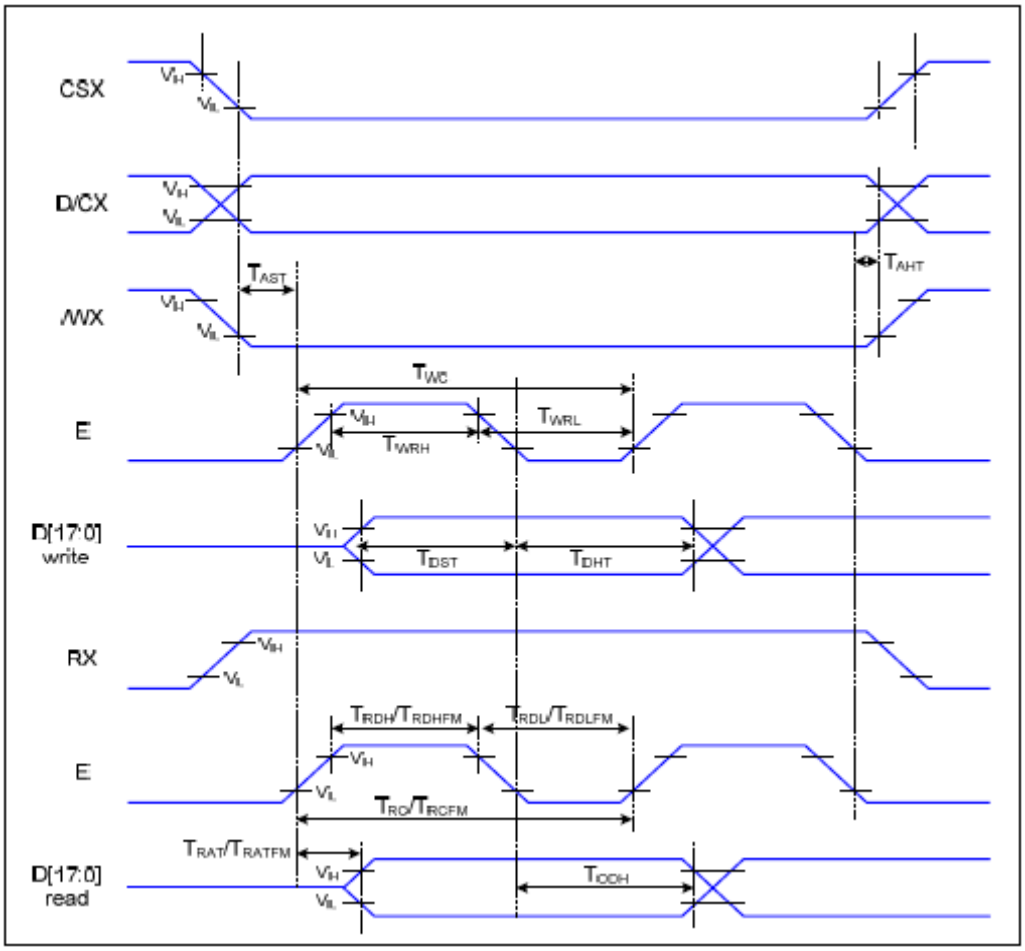
Rising and Falling Timing for I/O Signal



Write-to-Read and Read-to-Write Timing

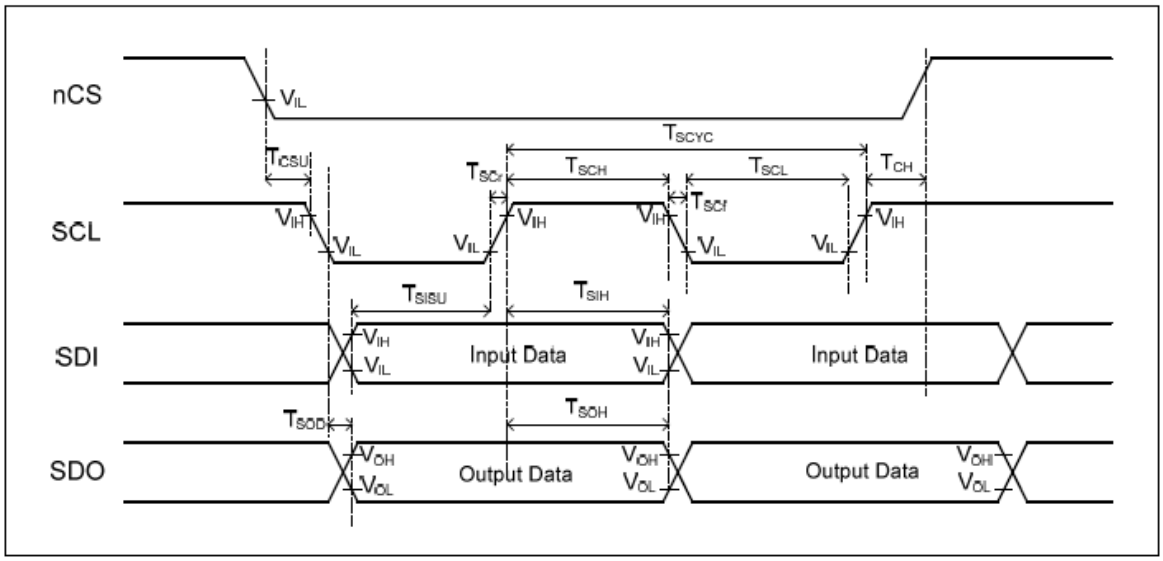
Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

6800 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus



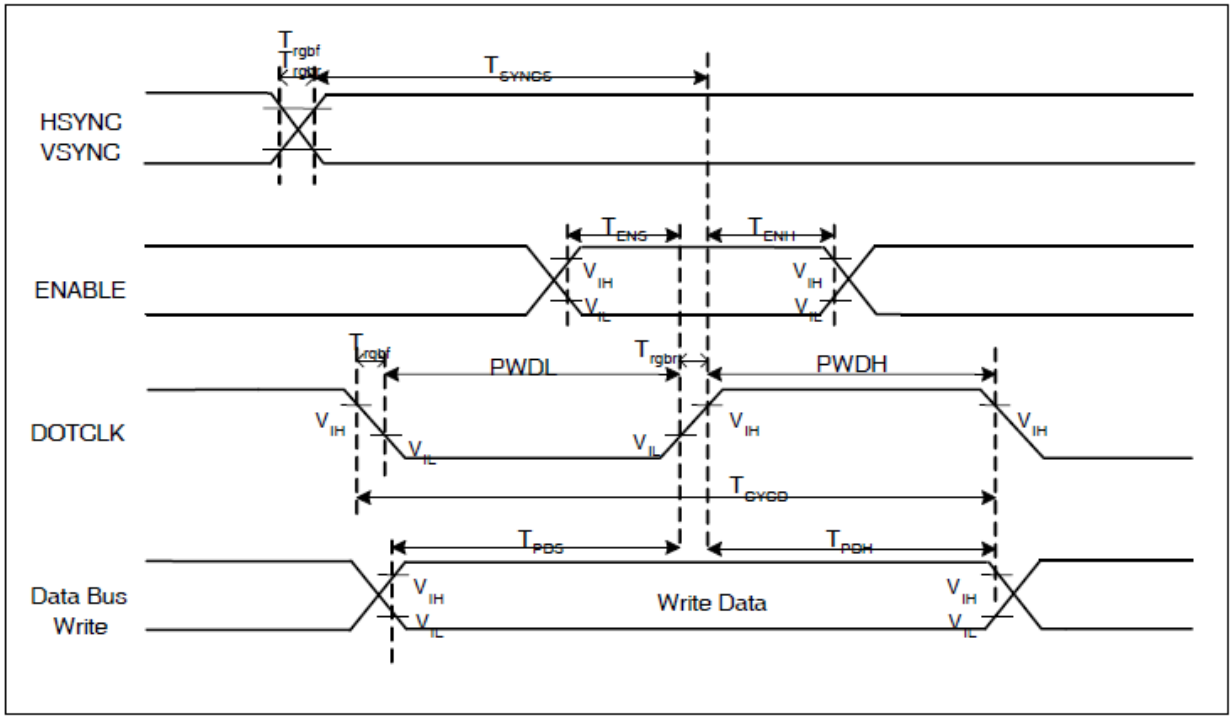
Signal	Symbol	Parameter	Min	Max	Unit	Description
DCX	T_{AST}	Address setup time	10		ns	-
	T_{AHT}	Address hold time (Write/Read)	5		ns	
E	T_{WC}	Write cycle	70		ns	
	T_{WRH}	Control pulse "H" duration	35		ns	
	T_{WRL}	Control pulse "L" duration	35		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	300		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	150		ns	
	T_{RDL}	Control pulse "L" duration (ID)	150		ns	
DB[17:0]	T_{DST}	Data setup time	10		ns	For maximum CL=30pF
	T_{DHT}	Data hold time	15		ns	
	T_{ODH}	Output disable time	50	--	ns	For minimum CL=8pF

Serial Data Transfer Interface Characteristics



Signal	Symbol	Parameter	Min	Max	Unit	Description
CSX	TCSU	Chip Select Setup Time	10		ns	-
	TCH	Chip Select Hold Time	50		ns	
SCL	TSCr ,TSCf	Serial clock rise/fall time		5	ns	
	TSCH	SCL "H" pulse width (Write)	40		ns	
	TSCH	SCL "H" pulse width (Read)	100		ns	
	TSCYC	Serial clock cycle (Write)	80		ns	
	TSCYC	Serial clock cycle (Read)	200		ns	
	TSCL	SCL "L" pulse width (Write)	40		ns	
	TSCL	SCL "L" pulse width (Read)	100		ns	
SDI	TSISU	Serial Input Data Setup Time	20		ns	
	TSIH	Serial Input Data Hold Time	20		ns	
SDO	TSOD	Serial Output Data Setup Time		100	ns	
	TSOH	Serial Output Data Hold Time	5		ns	

RGB Interface Characteristics



Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	TSYNCS	VSYNC, HSYNC Setup Time	0		ns	
	Trghr, Trghf	VSYNC, HSYNC Rise/Fall time		25	ns	
ENABLE	TENS	Enable Setup Time	10		ns	
	TENH	Enable Hold Time	10		ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	40		ns	
	PWDL	DOTCLK Low-level Pulse Width	40		ns	
	TCYCD	DOTCLK Cycle Time	100		ns	
	Trghr, Trghf	DOTCLK Rise/Fall time		25	ns	
DB	TPDS	PD Data Setup Time	10		ns	
	TPDH	PD Data Hold Time	40		ns	

18/16 Bits RGB Interface Timing Characteristics

Signal	Symbol	Parameter	MIN	MAX	Unit	Description
HSYNC, VSYNC	TSYNCS	VSYNC, HSYNC Setup Time	0		ns	
	Trghr, Trghf	VSYNC, HSYNC Rise/Fall time		25	ns	
ENABLE	TENS	Enable Setup Time	10		ns	
	TENH	Enable Hold Time	10		ns	
DOTCLK	PWDH	DOTCLK High-level Pulse Width	30		ns	
	PWDL	DOTCLK Low-level Pulse Width	30		ns	
	TCYCD	DOTCLK Cycle Time	80		ns	
	Trghr, Trghf	DOTCLK Rise/Fall time		25	ns	
DB	TPDS	PD Data Setup Time	10		ns	
	TPDH	PD Data Hold Time	30		ns	

6 Bits RGB Interface Timing Characteristics

7. Optical Characteristics:

Item		Symbol	Conditions	Specifications			Unit	Note
				Min	Typ	Max		
Transmittance		T(%)	-	-	5.0	-	-	-
Contrast Ratio		CR	θ=0 Normal Viewing angle	250	500	-		(1) (2)
Response time		TR+TF	-	-	10	20	ms	(1) (3)
Viewing angle	Hor.	Θx+	CR≧10	-	70	-	deg.	(4)
		Θx-		-	70	-		
	Ver.	Θy+		-	70	-		
		Θy-		-	60	-		

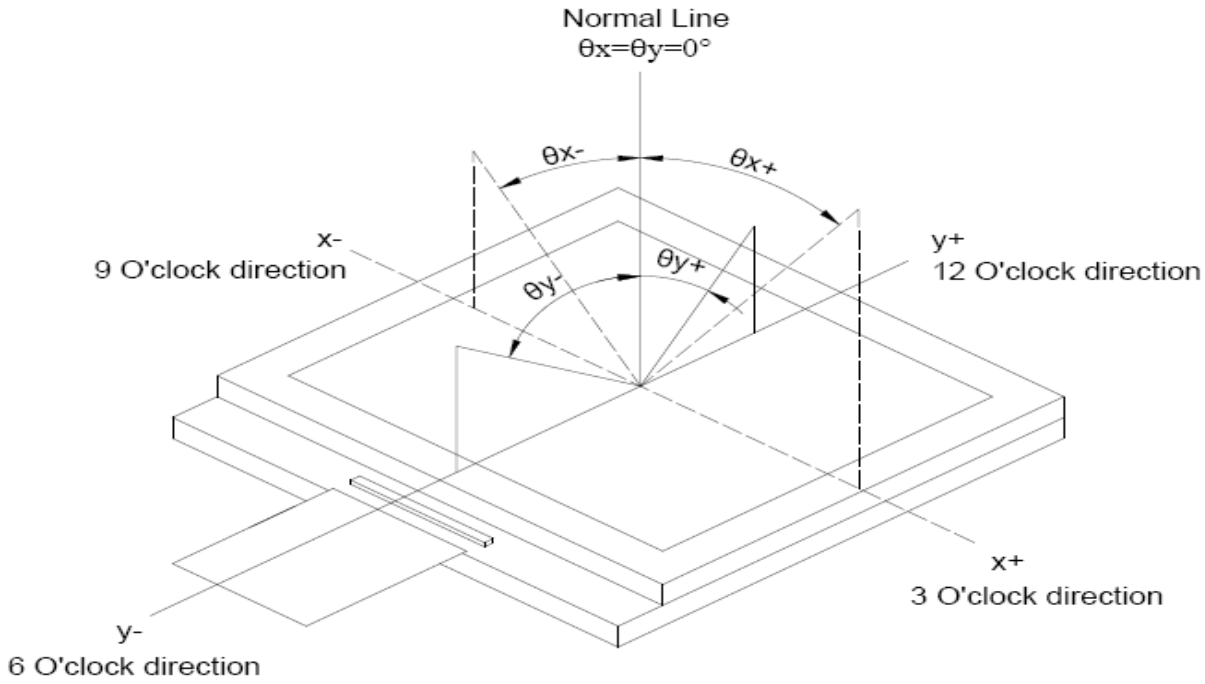
Measuring Condition

1. Measuring surrounding: dark room
2. Ambient temperature: 25±2℃
3. 30 min. Warm-up time.

Color of CIE Coordinate:

Item		Symbol	Condition	Min.	Typ.	Max.	Brightness
Chromaticity Coordinates (Transmissive)	Red	x	θ = φ = 0° LED Backlight Color Degree X=0.30 Y=0.30 Brightness =3000 cd/m²	0.543	0.593	0.643	40 cd/m²
		y		0.2952	0.3452	0.3952	
	Green	x		0.2671	0.3171	0.3671	210 cd/m²
		y		0.5383	0.5883	0.6383	
	Blue	x		0.0986	0.1486	0.1986	55 cd/m²
		y		0.0277	0.0777	0.1277	
	White	x		0.2276	0.2776	0.3276	150 cd/m²
		y		0.2483	0.2983	0.3483	

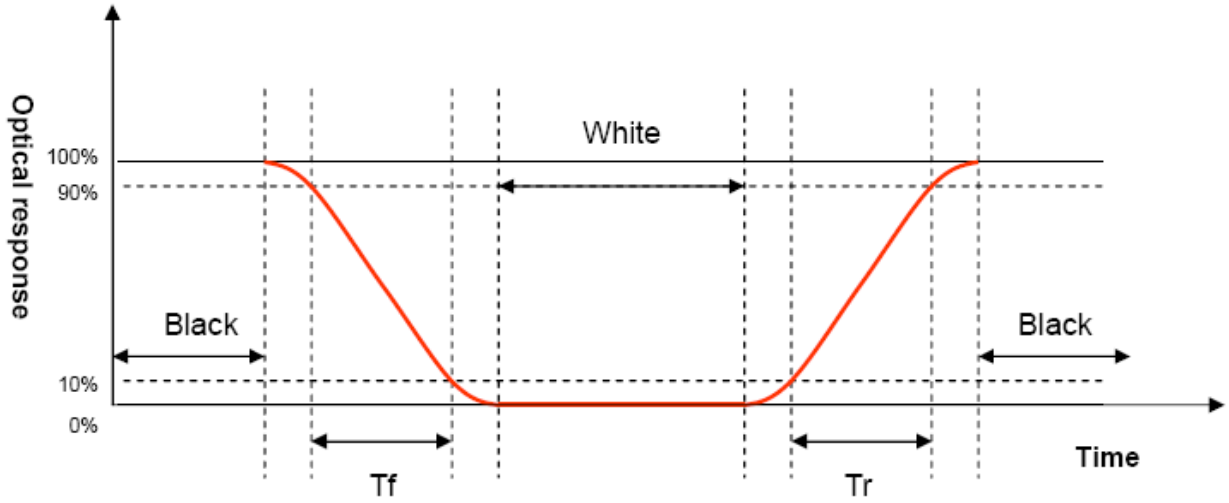
Note (1) Definition of Viewing Angle :



Note (2) Definition of Contrast Ratio(CR) :
measured at the center point of panel

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black}}$$

Note (3) Definition of Response Time : Sum of TR and TF



Note (4) Suggestion: LCD at the optima view direction is"12 O'clock " . When at the large angle, it is possible to see the grayscale inversion, for the reason that the best view direction by the human eye is"6 O'clock ".

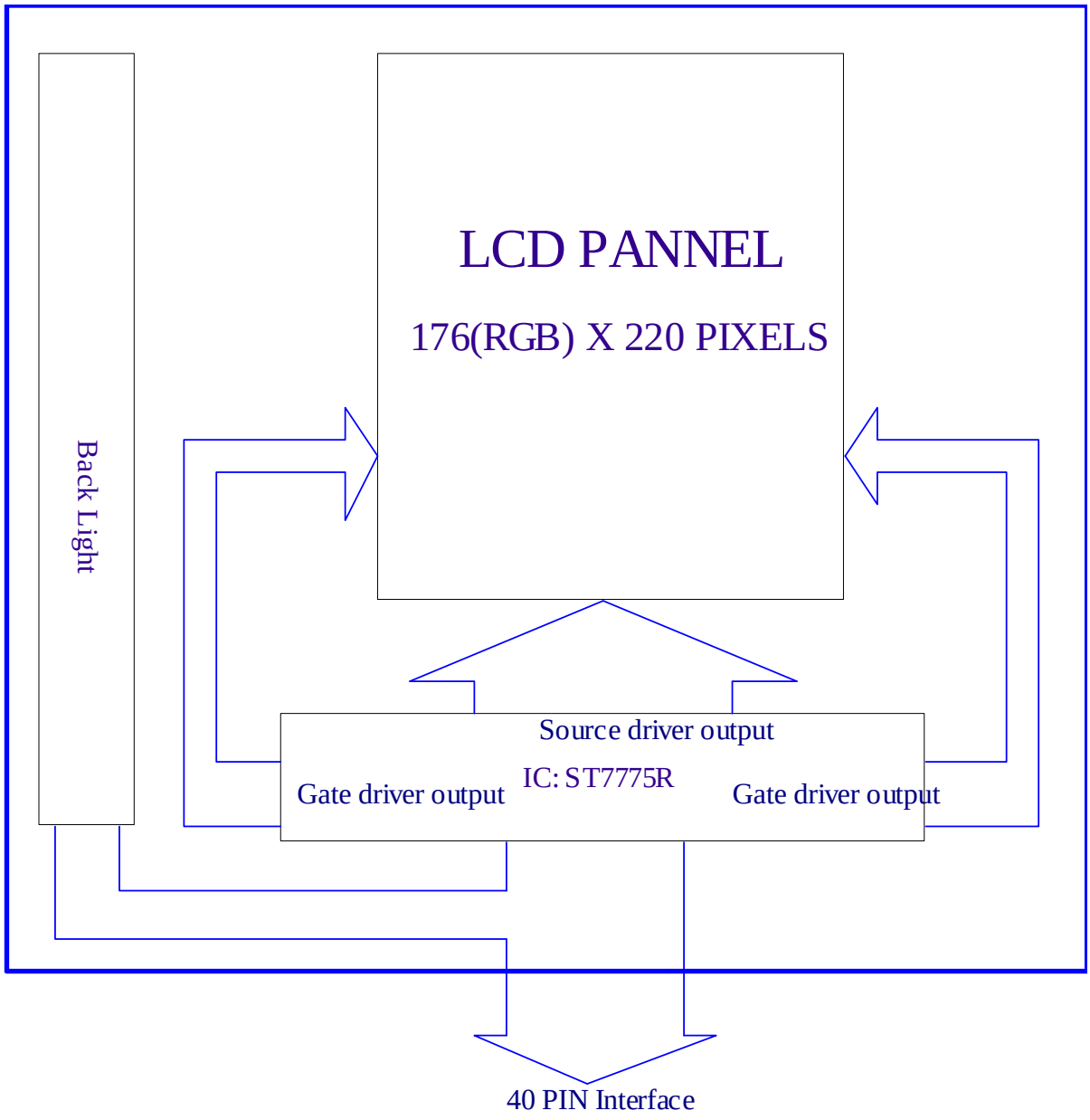
8. Interface Pin Assignment:

8-1 LCM FPC Interface

<table>
<tr><td>No.</td><td>Symbol</td><td>Function</td></tr>
<tr><td>1</td><td>GND</td><td>Power Ground</td></tr>
<tr><td>2</td><td>VCC</td><td>Power Supply for Analog, Digital System and Booster Circuit.</td></tr>
<tr><td>3</td><td>VCC</td><td>Power Supply for Analog, Digital System and Booster Circuit.</td></tr>
<tr><td>4</td><td>IOVCC</td><td>Power Supply for I/O System.</td></tr>
<tr><td>5~8</td><td>IM0~IM3</td><td>
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MCU Interface Mode</th><th>Data pin</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>68-16 bit</td><td>DB[17:10], DB[8:1]</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>68-8 bit</td><td>DB[17:10]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80-16 bit</td><td>DB[17:10], DB[8:1]</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80-8 bit</td><td>DB[17:10],</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>ID</td><td>24-bit SPI</td><td>CSX ,SCL ,SDI, SDO</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>9- bit SPI</td><td>CSX,SCL,SDA</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>8- bit SPI</td><td>CSX,SCL,SDA,DCX</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>68-18 bit</td><td>DB[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>68-9 bit</td><td>DB[17:9]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80-18bit</td><td>DB[17:0]</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80-9bit</td><td>DB[17:9]</td></tr>
<tr><td>1</td><td>1</td><td>--</td><td>--</td><td>Setting invalid</td><td></td></tr>
</table>
</td></tr>
<tr><td>9~26</td><td>DB0~DB17</td><td>MCU parallel interface data bus, -If not used, please fix this pin at GND level.</td></tr>
<tr><td>27</td><td>SDO</td><td>SPI interface output pin.
The data is outputted on the falling edge of the SCL signal.
If not used, please fix this pin at floating.</td></tr>
<tr><td>28</td><td>W/R(SCL)</td><td>Write enable in MCU parallel interface.
In SPI mode, this is used as SCL.</td></tr>
<tr><td>29</td><td>R/D</td><td>Read enable in 8080 MCU parallel interface.
If not used, please fix this pin at VCC or GND level.</td></tr>
<tr><td>30</td><td>SDI</td><td>SPI interface input pin.
The data is latched on the rising edge of the SCL signal.
In the 24-bit serial peripheral interface, this pin is used as input Pin.
In the 8/9-bit serial peripheral interface, this pin is used as bi-directional data pin.
If not used, please fix this pin at GND level.</td></tr>
<tr><td>31</td><td>RESET</td><td>This signal will reset the device and it must be applied to properly initialize the chip. Low active</td></tr>
<tr><td>32</td><td>ENABLE</td><td>Data enable signal for RGB interface operation.
Low: Select (access enabled), High: Not select (access disabled)
If not used, please fix this pin at VCC or GND level.</td></tr>
<tr><td>33</td><td>DOTCLK</td><td>Dot clock signal for RGB interface operation.
If not used, please fix this pin at GND level.</td></tr>
<tr><td>34</td><td>HSYNC</td><td>Horizontal (Line) synchronizing input signal for RGB interface operation.
If not used, please fix this pin at GND level.</td></tr>
</table>

35	VSYNC	Vertical (Frame) synchronizing input signal for RGB interface operation. If not used, please fix this pin at GND level.
36	CSX	Chip selection pin.
37	D/C(RS)	Display data/command selection pin in MCU interface. D/C=’1’: display data or parameter. D/C=’0’: command data. If not used, please fix this pin at VCC or GND level.
38	NC	No Connect.
39	LEDA	LED Light, anode
40	LEDK	LED Light, cathode

9. Block Diagram:



10. Backlight:

1. Standard Lamp Styles (Edge Lighting Type):
The LED chips are distributed over the edge light area of the illumination unit, which gives the less power consumption:

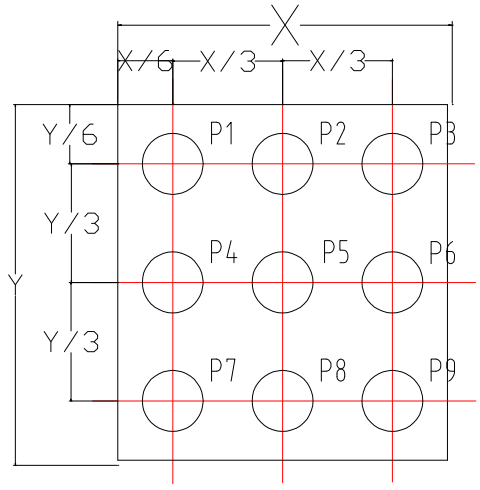
2. The Main Advantages of the LED Backlight are as following:
2.1 The brightness of the backlight can simply be adjusted.
By a resistor or a potentiometer.

3. Data About LED Backlight: (Ta=25°)

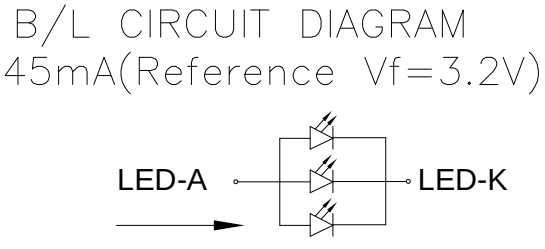
PARAMETER	Sym.	Min.	Typ.	Max.	Unit	Test Condition	Note
Supply Voltage	V	2.9	3.2	3.5	V	If=45mA	
Reverse Voltage	VR	-	-	5	V	-	
Luminous Intensity for LCM	Iv	100	150	-	Cd/m^2	If=45mA	2
Uniformity for LCM	-	70	-	-	%		3
Life Time	-	-	50000	-	Hr.		4
Color	White						

NOTE:
1. Backlight Only
2. Average Luminous Intensity of P1-P9
3. Uniformity = Min/Max * 100%
4. LED life time defined as follows: The final brightness is at 50% of original brightness

Measured Method: (X*Y: Light Area)



Internal Circuit Diagram



11. Standard Specification for Reliability:

11 - 1 Standard Specifications for Reliability of LCD Module

No	Item	Description
01	High temperature operation	The sample should be allowed to stand at 70℃ for 120 hours under driving condition and then returning it to normal temperature condition, and allowing it stand for 2 hours.
02	Low temperature operation	The sample should be allowed to stand at -20℃ for 120 hours under driving condition and then returning it to normal temperature condition, and allowing it stand for 2 hours.
03	High temperature storage	The sample should be allowed to stand at 80℃ for 240 hours under no-load condition, and then returning it to normal temperature condition, and allowing it stand for 2 hours.
04	Low temperature storage	The sample should be allowed to stand at -30℃ for 240 hours under no-load condition, then returning it to normal temperature condition, and allowing it stand for 2 hours.
05	Moisture storage	The sample should be allowed to stand at 60℃,90%RH MAX for 240 hours under no-load condition, then taking it out and drying it at normal temperature for 2 hours.
06	Thermal shock storage	The sample should be allowed to stand the following 10 cycles : -30℃ for 30 minutes → normal temperature for 5 minutes → +80℃ for 30 minutes → normal temperature for 5 minutes, as one cycle.
07	Packing vibration	Frequency range : 10Hz ~ 55Hz Amplitude of vibration : 1.5mm Sweep time: 12 min X,Y,Z 2 hours for each direction.
08	Packing drop test	According to ISTA 1A 2001.

09	Electrical Static Discharge	Air: ±4KV 150pF/330Ω 5 times
		Contact: ±2KV 150pF/330Ω 5 time

*Sample size for each test item is 3~5pcs

11 - 2. Testing Conditions and Inspection Criteria

For the final test the testing sample must be stored at room temperature for 24 hours, after the tests listed in Table 11-1, Standard specifications for Reliability have been executed in order to ensure stability.

No	Item	Test Model	In section Criteria
01	Current Consumption	Refer To Specification	The current consumption should conform to the product specification.
02	Contrast	Refer To Specification	After the tests have been executed, the contrast must be larger than half of its initial value prior to the tests.
03	Appearance	Visual inspection	Defect free.

11- 3. MTBF

MTBF	Functions, performance, appearance, etc. shall be free from remarkable deterioration within 50,000 hours under ordinary operating and storage conditions room temperature (25±5℃), normal humidity (50±10% RH), and in area not exposed to direct sun light.

12. Specification of Quality Assurance:

12-1. Purpose

This standard for Quality Assurance should affirm the quality of LCD module products to supply to purchaser by YEEBO CORPORATION (Supplier).

12-2. Standard for Quality Test

a. Inspection:

Before delivering, the supplier should take the following tests, and affirm the quality of product.

b. Electro-Optical Characteristics:

According to the individual specification to test the product.

c. Test of Appearance Characteristics:

According to the individual specification to test the product.

d. Test of Reliability Characteristics:

According to the definition of reliability on the specification for testing products.

e. Delivery Test:

Before delivering, the supplier should take the delivery test.

(i) Test method: According to MIL-STD105E.General Inspection Level Ⅱ take a single time.

(ii) The defects classify of AQL as following:

Major defect: AQL = 0.65

Minor defect: AQL = 2.5

Total defects: AQL = 2.5

12-3. Non- conforming Analysis & Deal With Manners

a. Non- conforming Analysis:

(i) Purchaser should supply the detail data of non- conforming sample and the non-conforming.

(ii) After accepting the detail data from purchaser, the analysis of non- conforming should be finished in two weeks.

(iii) If supplier can not finish analysis on time, must announce purchaser before 3 days.

b. Disposition of non- conforming:

(i) If find any product defect of supplier during assembly time, supplier must change the good product for every defect after recognition.

(ii) Both supplier and customer should analyze the reason and discuss the disposition of non- conforming when the reason of nonconforming is not sure.

12-4. Agreement items

Both sides should discuss together when the following problems happen.

a. There is any problem of standard of quality assurance, and both sides should think that must be modified.

b. There is any argument item which does not record in the standard of quality assurance.

c. Any other special problem.

12-5. Standard of The Product Appearance Test

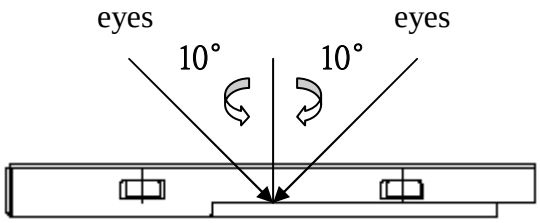
a. Manner of appearance test:

(i) The test must be under 20W × 2 or 40W fluorescent light, and the distance of view must be at 30±5cm.

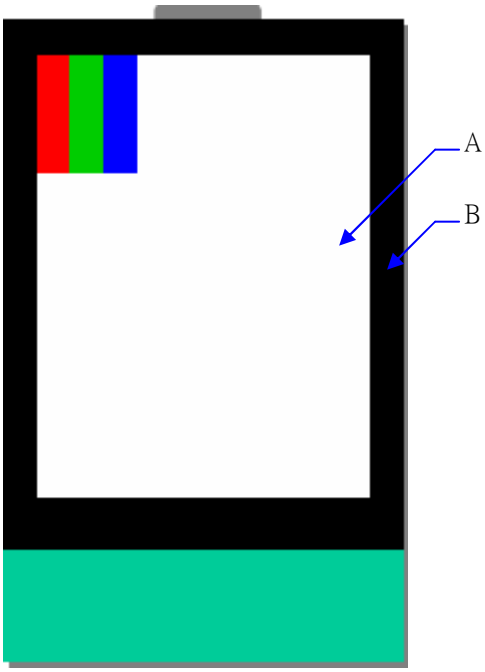
(ii) When test the model of transmissive product must add the reflective plate.

(iii)The test direction is base on around 10° of vertical line.

(iiii)Temperature: 25±5℃ Humidity: 60±10%RH



(iv) Definition of area:



A. Area: Viewing area.

B. Area: Out of viewing area.
(Outside viewing area)

b. Basic principle:

(i) It will accord to the AQL when the standard can not be described.

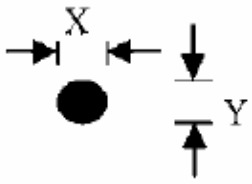
(ii) The sample of the lowest acceptable quality level must be discussed by both supplier and customer when any dispute happened.

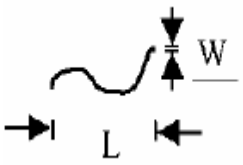
(iii) Must add new item on time when it is necessary.

c. Standard of inspection: (Unit: mm)

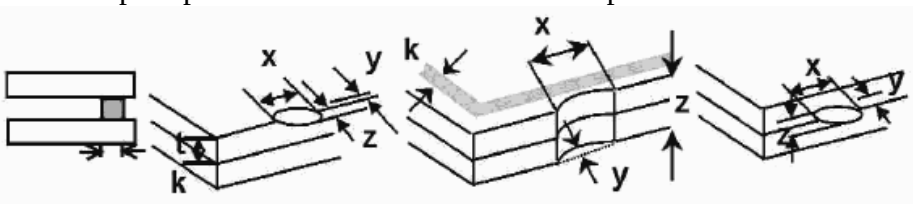
12-6. Inspection specification

Defect out of viewing area can be neglected.

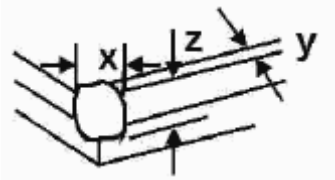
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>01</td><td>Electrical Testing</td><td>1.1 Missing vertical, horizontal segment, segment contrast defect.
1.2 Missing character, dot or icon.
1.3 Display malfunction.
1.4 No function or no display.
1.5 Current consumption exceeds product specifications.
1.6 LCD viewing angle defect.
1.7 Mixed product types.
1.8 Flicker</td><td>0.65</td></tr>
<tr><td>02</td><td>Black or White spots or Bright spots or Color spots on LCD (Display only)</td><td>2.1 White and black or color spots on display ≦ 0.25mm, no more than Five spots.
2.2 Densely spaced: No more than three spots within 3mm.</td><td>2.5</td></tr>
<tr><td rowspan="2">03</td><td rowspan="2">LCD and Touch Panel black spots, white spots, contamination (non – display)</td><td>3.1 Round type: As following drawing
Φ = (X+Y) / 2
 

<table>
<tr><th>Size(mm)</th><th>Acceptable Q'ty</th></tr>
<tr><td>Φ≦0.10</td><td>Accept no dense</td></tr>
<tr><td>0.10< Φ≦0.20</td><td>2</td></tr>
<tr><td>0.20< Φ≦0.25</td><td>2</td></tr>
<tr><td>0.25< Φ≦0.30</td><td>1</td></tr>
<tr><td>0.30< Φ</td><td>0</td></tr>
</table>
* Densely spaced: No more than two spots within 3mm.</td><td>2.5</td></tr>
<tr><td>3.2 Line type: (As following drawing)
 

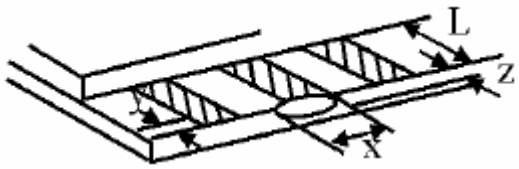
<table>
<tr><th>Length(mm)</th><th>Width(mm)</th><th>Acceptable Q'ty</th></tr>
<tr><td>---</td><td>W≦0.02</td><td>Accept no dense</td></tr>
<tr><td>L≦3.0</td><td>0.02<W≦0.05</td><td rowspan="2">2</td></tr>
<tr><td>L≦2.5</td><td>0.03<W≦0.08</td></tr>
<tr><td>---</td><td>0.08<W</td><td>Rejection</td></tr>
</table>
* Densely spaced: No more than two lines within 3mm.</td><td>2.5</td></tr>
</table>

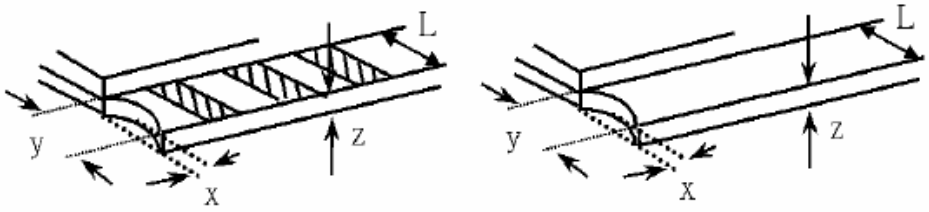
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>04</td><td>Polarizer bubbles</td><td>If bubbles are visible, judge using black spot specifications, not easy to find, must check in specify direction
<table>
<tr><td>Size Φ(mm)</td><td>Acceptable Q'ty</td></tr>
<tr><td>Φ≦0.20</td><td>Accept no dense</td></tr>
<tr><td>0.20< Φ≦0.50</td><td>3</td></tr>
<tr><td>0.50< Φ≦1.00</td><td>2</td></tr>
<tr><td>1.00< Φ</td><td>0</td></tr>
<tr><td>Total Q’ty</td><td>3</td></tr>
</table></td><td>2.5</td></tr>
<tr><td>05</td><td>Scratches</td><td>Follow NO.3 -2 Line Type.</td><td></td></tr>
<tr><td>06</td><td>Chipped glass</td><td>Symbols:
x: Chip length y: Chip width z: Chip thickness
k: Seal width t: Glass thickness a: LCD side length
L: Electrode pad length
6.1 General glass chip:
6.1.1 Chip on panel surface and crack between panels:
 

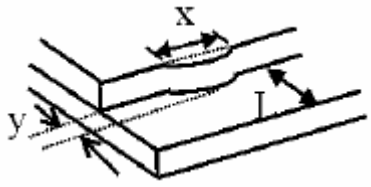
<table>
<tr><td>z: Chip thickness</td><td>y: Chip width</td><td>x: Chip length</td></tr>
<tr><td>Z≦1/2t</td><td>Not over viewing area</td><td>x≦1/8a</td></tr>
<tr><td>1/2t< z≦2t</td><td>Not exceed 1/3k</td><td>x≦1/8a</td></tr>
</table>
⊙ Unit: mm
⊙ If there are 2 or more chips, x is the total length of each chip

6.1.2 Corner crack:
 

<table>
<tr><td>z: Chip thickness</td><td>y: Chip width</td><td>x: Chip length</td></tr>
<tr><td>Z≦1/2t</td><td>Not over viewing area</td><td>x≦1/8a</td></tr>
<tr><td>1/2t< z≦2t</td><td>Not exceed 1/3k</td><td>x≦1/8a</td></tr>
</table>
⊙ Unit: mm
⊙ If there are 2 or more chips, x is the total length of each chip</td><td>2.5</td></tr>
</table>

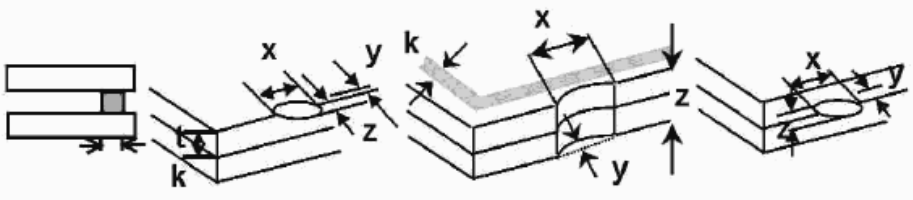
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>07</td><td>Glass crack</td><td>
Symbols:
x: Chip length y: Chip width z: Chip thickness
k: Seal width t: Glass thickness a: LCD side length
L: Electrode pad length
7.2 Protrusion over terminal:
7.2.1 Chip on electrode pad:


<table>
<tr><th>y: Chip width</th><th>x: Chip length</th><th>z: Chip thickness</th></tr>
<tr><td>y≦0.5mm</td><td>x≦1/8a</td><td>0< z≦t</td></tr>
</table>
7.2.2
Non-conductive portion:


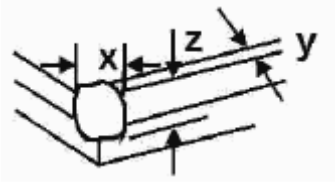
<table>
<tr><th>y: Chip width</th><th>x: Chip length</th><th>z: Chip thickness</th></tr>
<tr><td>y≦L</td><td>x≦1/8a</td><td>0< z≦t</td></tr>
</table>
⊙ If there chipped area touches the ITO terminal, over 2/3 of the ITO must remain and be inspected according to electrode terminal specifications.
⊙ If the product will be heat sealed by the customer, the alignment mark must mot be damaged.
7.2.3 Substrate protuberance and internal crack


<table>
<tr><th>y: width</th><th>x: length</th></tr>
<tr><td>y≦1/3L</td><td>X≦a</td></tr>
</table>
</td><td>2.5</td></tr>
</table>

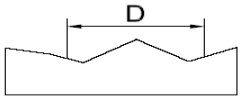
NO	Item	Criterion	AQL
08	Cracked glass	The LCD with extensive crack is not acceptable.	2.5
09	Backlight elements	9.1 Illumination source flickers when lit. 9.2 Spots or scratches that appear when lit must be judged. Using LCD spot, lines and contamination standards. 9.3 Backlight doesn't light or color is wrong.	2.5 2.5 0.65
10	Bezel	Bezel must comply with product specifications.	2.5
11	PCB、COB	11.1COB seal may not have pinholes larger than 0.2mm or contamination. 11.2 COB seal surface may not have pinholes through to the IC. 11.3 The height of the COB should not exceed the height indicated in the assembly diagram. 11.4 There may not be more than 2mm of sealant outside the seal area on PCB. And there should be no more than three places. 11.5 Parts on PCB must be the same as on the production characteristic chart, There should be no wrong parts, missing parts or excess parts. 11.6 The jumper on the PCB should conform to the product characteristic chart.	2.5 2.5 2.5 2.5 0.65 0.65
12	FPC	12.1 FPC terminal damage ≦ 1/2 FPC terminal width and can not affect the function , we judge accept. 12.2 FPC alignment hole damage ≦ 1/2 alignment area and can not affect the function , we judge accept.	2.5 2.5
13	Soldering	13.1 No cold solder joints, missing solder connections, oxidation or icicle. 13.2 No short circuits in components on PCB or FPC.	2.5 0.65

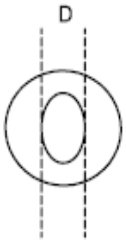
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>14</td><td>Touch Panel Chipped glass</td><td>
Symbols:
x: Chip length y: Chip width z: Chip thickness
k: Seal width t: Touch Panel Total thickness a: LCD side length
L: Electrode pad length
14.1 General glass chip:
14.1.1 Chip on panel surface and crack between panels:


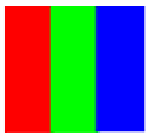
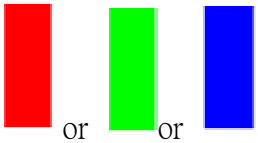
<table>
<tr><th>z: Chip thickness</th><th>y: Chip width</th><th>x: Chip length</th></tr>
<tr><td>Z≦t</td><td>≦1/2 k and not over viewing area</td><td>x≦1/8a</td></tr>
</table>
⊙ Unit: mm
⊙ If there are 2 or more chips, x is the total length of each chip

14.1.2 Corner crack:


<table>
<tr><th>z: Chip thickness</th><th>y: Chip width</th><th>x: Chip length</th></tr>
<tr><td>z≦t</td><td>≦1/2 k and not over viewing area</td><td>x≦1/8a</td></tr>
</table>
⊙ Unit: mm
⊙ If there are 2 or more chips, x is the total length of each chip
</td><td>2.5</td></tr>
</table>

<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>15</td><td>Touch Panel(Fish eye、dent and bubble on film)</td><td>
<table>
<tr><th>SIZE(mm)</th><th>Acceptable Q’ty</th></tr>
<tr><td>Φ≦0.2</td><td>Accept no dense</td></tr>
<tr><td>0.2< D ≦0.4</td><td>5</td></tr>
<tr><td>0.4< D ≦0.5</td><td>2</td></tr>
<tr><td>0.5< D</td><td>0</td></tr>
</table>




</td><td>2.5</td></tr>
<tr><td>16</td><td>Touch Panel Newton ring</td><td>Newton ring dimension ≦ 1/2 touch panel area and not affect font and line distortion(≦2.5%) , it is acceptable.</td><td>2.5</td></tr>
<tr><td>17</td><td>Touch Panel Linearity</td><td>Less than 2.5% is acceptable.</td><td>2.5</td></tr>
<tr><td>18</td><td>LCD Ripple</td><td>Touch the touch panel , can not see the LCD ripple.
Pen: R 1.0mm silicon rubber.
Operation Force: 80g</td><td>2.5</td></tr>
<tr><td>19</td><td>General appearance</td><td>19.1 Pin type must match type in specification sheet.
19.2 LCD pin loose or missing pins.
19.3 Product packaging must the same as specified on packaging specification sheet.
19.4 Product dimension and structure must conform to product specification sheet.</td><td>0.65
0.65
0.65
0.65</td></tr>
<tr><td>20</td><td>Definition of Pixel</td><td>Pixel : Group of Three Sub-pixels (Red, Green ,Blue):
 
Dot : Red or Green or Blue
 
or or
Dot : Any sub-pixel
Bright Dot Defects
Dots (sub-pixels) on display which is bright in the picture and visible at Black Pattern.</td><td></td></tr>
</table>

Dark Dot Defects
Dots(sub-pixels) on display which is dark in the picture and visible at Red/Green/Black/White Pattern.
Neighbour Dot Defects
Two or three neighbour dots (dot: sub-pixel) cluster(R&G,G&B,B&R,or R&G&B).Dot Defects Inspection Criteria
NOTE : Dot out of VA can be ignored.

Items	Inspection Criteria	
	Details	Allowed quantity
Bright Dot	Not Neighbour Dot	2
Dark Dot	Not Neighbour Dot	3
Total acceptable Qty		5

- Size of dot defect is larger than half of one sub-pixel.

13. Handling Precaution:

13-1 Handling of LCM

- Don't give external shock.
- Don't apply excessive force on the surface.
- Liquid in LCD is hazardous substance. Must not lick and swallow. when the liquid is attach to your hand, skin, cloth etc. Wash it out thoroughly and immediately.
- Don't operate it above the absolute maximum rating.
- Don't disassemble the LCM.
- The operators should be grounded whenever he/she comes into contact with the module. Never touch any of the conductive parts such as the LSI pads,the copper leads on the PCB and the interface terminals with any parts of the human body.
- The modules should be kept in antistatic bags or other containers resistant to static for storage.
- The module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

13-2 Storage

- Store in an ambient temperature of 25±10℃, and in a relative humidity of 50±10%RH. Don't expose to sunlight or fluorescent light.
- Storage in a clean environment, free from dust, active gas, and solvent.
- Store in anti-static electricity container.
- Store without any physical load.

13-3 Soldering

- Use only soldering irons with proper grounding and no leakage.
- Iron: No higher than 280±10℃ and less than 3 sec during Hand soldering.
- Rewiring: no more than 2 times.

14. Guarantee:

Our products could meet requirements of the environment.
YB's RoHS is introduce European Union Directive 2011/65/EU (ROHS) Requirements and update.